Researchers develop multilevel memory for consumer electronics

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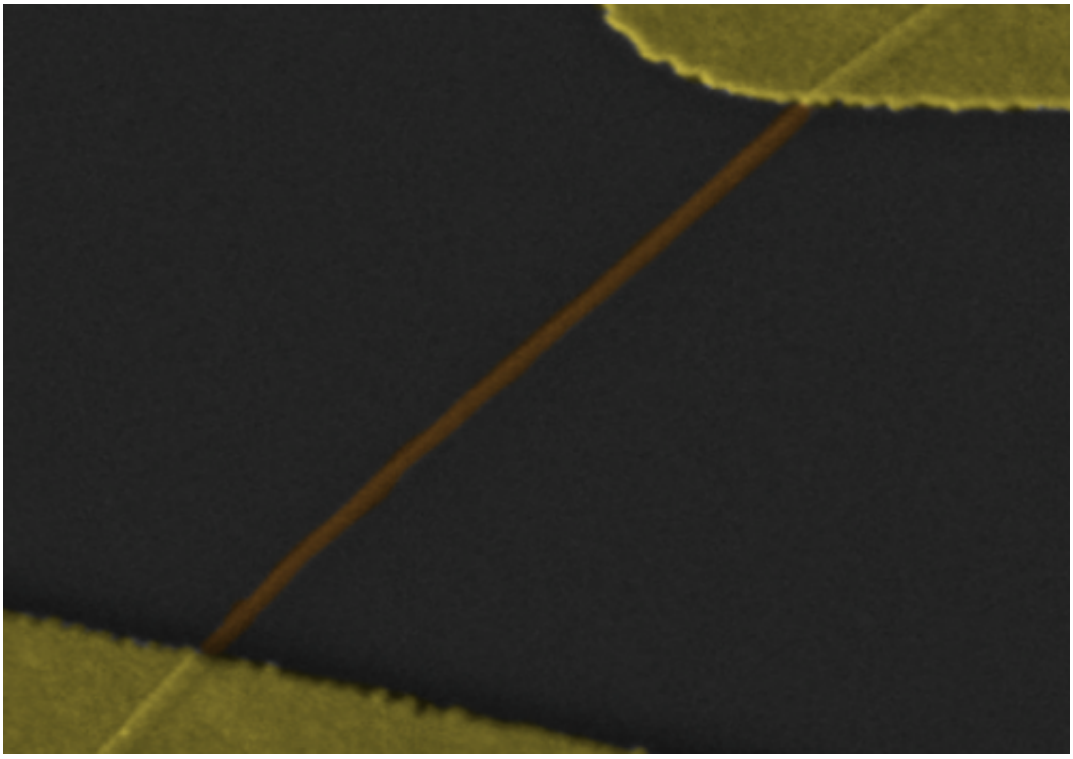

A titanium oxide nanowire acts as both a diode and a memristor

Researchers at AMBER, the Science Foundation Ireland funded materials science centre, and the School of Chemistry, Trinity College Dublin, have developed a solution to increase the speed interaction between processor and memory in computers and other electronic devices.

Instead of each memory cell storing just a single piece or 'bit' of information, the team - led by Professor John Boland with researchers Curtis O'Kelly and Jessamyn Fairfield has developed a multilevel memory in which it is possible to programme a number of stored bits into a single cell. Multilevel memory increases communication speed by reducing the number of memory cells.

Whether your favorite app runs on a mobile phone or a supercomputer, performance no longer depends solely on the brain power or so-called processor speed. To function, the processor has to communicate efficiently with memory on the chip. The properties of the metal wires connecting the processor and memory provide a fundamental speed limit.

Professor John Boland, AMBER, explained: "Processors and memory communicate using the clunky language of binary code. Conventional on-chip memory stores information as '1's' and '0's', which reflects the presence or absence of charge at the memory location. For example, 2014 in binary language requires 11 cells of memory. It take time for the computer to access such a large number of cells and so the overall performance is impaired. The new process reduces the number of cells required."

The scheme proposed by the AMBER researchers operates on a different principle; the resistance to charge flow, known as resistive memory which ultimately leads to more streamlined processing with fewer cells but with each having multiple memory levels. A particular advantage of the new approach is that it is possible to arbitrarily tune the number of memory levels within each cell.

"The discovery opens up a host of possibilities for the consumer leading to smaller, cheaper and faster electronics. Having demonstrated six memory levels per cell, we believe the technology can be developed to

display even more memory levels per cell. A memory language with greater density can increase the efficiency and speed of desktop and mobile technology by reducing the number of memory locations," said Professor Boland.

"Further research will be focused on integrating this technology with existing industry fabrication capabilities, so that society can continue to reap the benefits with new and improved technology," Professor Boland concluded.

More information: The paper, A Single Nanoscale Junction with Programmable Multilevel Memory is available at: pubs.acs.org/doi/abs/10.1021/nn505139m

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