Spintronic interconnect modeling for beyond-CMOS computing

June 4 2014, by Dan Francisco

Georgia Institute of Technology researchers collaborating with and sponsored by Intel Corporation through the Semiconductor Research Corporation (SRC) have developed a physics-based modeling platform that advances spintronics interconnect research for beyond-CMOS computing.

Spin-logic aims at reducing power consumption of electronic devices, thereby improving battery life and reducing energy consumption in computing for a whole range of electronic product applications from portable devices to data centers.

"After more than four decades of exponential growth in the performance of electronic integrated circuits, it is now apparent that improving the energy efficiency of computing is a primary challenge," said Ian A. Young, a collaborator and co-author of the research and a Senior Fellow at Intel Corporation. "There is a global search for information processing elements that use computational state variables other than electronic charge, and these devices are being sought to bring in new functionalities and further lower the power dissipation in computers."

One of the main motivations behind the search for a next-generation computing switch beyond CMOS (complementary metal oxide semiconductor) devices is to sustain the advancement of Moore's Law. Nanomagnetic/spintronic devices provide a complementary option to electronics. The added functionality of this option includes the non-volatility of information on-chip, which is in essence a combination of

logic and memory functions. However, to benefit from the increase in density of the on-chip devices, there has to be adequate connectivity among the switches—which is the focus of the Georgia Tech research.

Among the potential alternatives, devices based on nanoscale magnets in the field of spintronics have received special attention thanks to their advantages in terms of robustness and enhanced functionality. Magnets are non-volatile: their state remains even if the power to the circuit is switched off. Thus, the circuits do not consume power when not used—a very desirable property for modern tablets and smart phones.

One of the most important aspects of any new information processing element is how fast and power efficient they can communicate over an interconnect system with one another. In today's CMOS chips, more energy is consumed communicating between transistor logic functions than actually processing of information. The Georgia Tech research has therefore focused on this important aspect of communicating between spin-logic devices and demonstrates that interconnects are an even more important challenge for beyond-CMOS switches.

To analyze spintronic interconnects, the Georgia Tech team and their Intel collaborators have developed compact models for spin transport in copper and aluminum—taking into account the scattering at wire surfaces and grain boundaries that become quite dominant at nanoscale dimensions. The research team has also developed compact models for the nanomagnet dynamic, electronic and spintronic transport through magnet to non-magnet interfaces, electric currents and spin diffusion. These models are all based on familiar electrical elements such as resistors and capacitors and can therefore be analyzed using standard circuit simulation tools such as SPICE.

"This work is showing the way for how spintronics can create energy-efficient computation by including not only the spin logic functional

circuit blocks, but also the interconnect system parameters," said Jon Candelaria, director of Interconnect and Packaging Sciences at SRC. "This will help establish a much more realistic and accurate prediction of computing performance and power with spintronics."

More information: The research paper was presented at the IEEE Int. Interconnect Technology Conference on May 24 in San Jose, Calif., (www.iitc-conference.org/novel-systems-ii.html).

Provided by Semiconductor Research Corporation

Citation: Spintronic interconnect modeling for beyond-CMOS computing (2014, June 4) retrieved 11 July 2024 from https://phys.org/news/2014-06-spintronic-interconnect-beyond-cmos.html