Samsung's 14nm FinFET process technology ecosystem for mobile consumer and IT infrastructure

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Stating that not all FinFETs are created equal, Samsung Electronics today announced that the IP and design enablement ecosystem for its foundry's 14nm FinFET process technology is firmly in place as customers begin their early design work. Highlighting this fact, Samsung will be demonstrating a 14nm FinFET system-on-chip (SoC) reference board at the 51st Annual Design Automation Conference in San Francisco, June 2-4, Booth #819.

"To ease customers design risks moving to 14nm FinFET, we need to have all the elements of the design ecosystem optimized well in advance," said Dr. Shawn Han, vice president of foundry marketing, Samsung Electronics. "We are pleased to work with the industry's leading IP and design enablement companies. Our early work at this advanced node will allow our customers to bring their next-generation SoCs to the market quickly while taking full advantage of the benefits of our 14nm FinFET technology."

Samsung's foundry offering has focused its 14nm FinFET ecosystem efforts with key IP partners. Collaboration specifically around optimal Fin-based design infrastructure and early FinFET IP development has resulted in foundation libraries and advanced IP suite. On the enablement side, Samsung, with its EDA partners, has worked to optimize 3D device modeling, extraction solutions, and design verification as well as Design for Manufacturing (DFM) solutions. The

result of which is the 14nm FinFET reference board that will be on display at DAC 2014.

ARM® Artisan® physical IP for Samsung's 14nm FinFET process technology is now available for SoC designers and is the result of years of collaboration between ARM and Samsung. This partnership to develop foundation IP began with 45nm technology, leading to 32/28nm High-K Metal Gate (HKMG). This long-term collaboration has resulted in an optimized physical IP solution that provides greatly improved performance, lower leakage, and superior dynamic power characteristics. When used with the ARM Cortex® processors, this foundation IP enables a new generation of leading-edge, energy-efficient products for a wide range of markets that extends from mobile computing to new and emerging markets.

Through tight collaboration with Cadence, Samsung offers a full RTL-to-signoff flow that is power-, performance- and area-optimized for the 14nm FinFET process. This flow has been used to implement multiple early tapeouts on the process, including the first announced ARM processor tapeout in December 2012. Cadence provides a complete methodology for custom and digital design, place-and-route, extraction, timing, physical verification and DFM, including support for the Cadence Virtuoso and Encounter platforms through SKILL-based PDKs, EDI System and QRC extraction tech files and Physical Verification System rule decks.

Mentor is supporting Samsung's 14nm FinFET process technology with its Manufacturing Analysis and Scoring (MAS) deck, which prioritizes different DFM effects and makes recommendations on how to modify the design. Sign-off enabling for 14nm FinFET process technology also includes decks for design rule checking with double patterning and pattern matching-based verification, layout vs. schematic checking, lithography friendly design, and DFM with advanced fill.

The entire Synopsys Galaxy Design Platform is broadly supported on Samsung's 14nm FinFET process, for design tasks ranging from custom design through final place-and-route and signoff of complex SoCs. The Galaxy Design Platform tools, Samsung Foundry 14nm FinFET PDKs and associated tool usage have been tuned to deliver optimal results for SoC designers targeting the power and performance benefits of FinFET technology. Synopsys and Samsung have also proven the process, tool capabilities and IP in silicon via a series of complex SoCs which included both high performance processors and Synopsys-developed IP, including the recently certified DesignWare USB 3.0 femtoPHY.

Silicon-based PDK Availability

With process design kit of 14nm FinFET process technology available to customers today, customers can start designing with silicon-based SPICE models, extraction decks, design rule manuals and technology files that have been developed based on silicon results from 14nm FinFET test chips run in Samsung's state of art 300mm fabs. The PDK includes router tech files and other design enablement features to support the new 3-dimensional FinFET device structures, middle of line (MOL), and double patterning enablement used in the back end of line (BEOL) process. The investments that Samsung is making into the entire ecosystem at 14nm will give customers early access to all elements of the design infrastructure to accelerate their chip development.

Provided by Samsung