

# Record ADC for next-generation software defined radio

June 11 2014, by Hanne Degans

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Nanoelectronics research centre imec will present at this week's VLSI circuits symposium 2014 (Honolulu, June 13) a low power pipelined SAR (successive-approximation register) ADC (analog to digital converter) in 28nm digital CMOS with record resolution, speed and power performance. The novel ADC targets wireless receivers for next-generation software defined radio, including wireless standards such as LTE-advanced and the emerging generation of Wi-Fi (IEEE802.11ac).

In a software defined radio, the ADC needs high speed, high resolution and high [power](#) efficiency in a dynamic solution, supporting high, as well as low bandwidth standards. The pipelined SAR ADC developed by imec and Renesas Electronics achieves an excellent peak SNDR (signal to noise distortion ratio) of 70.7dB at a speed as high as 200MS/s while consuming only 2.3mW at 0.9V supply voltage. Moreover, the implementation in 28nm digital CMOS not only adds to its area and [power efficiency](#), but also supports digitalization of the radio.

"This novel ADC architecture is an important achievement in imec's R&D program on future wireless technologies, focusing on the development of highly flexible software-defined radios that support high bandwidth and well as low bandwidth standards," commented Liesbet Van der Perre, program director wireless technologies at imec. "The architecture is based on prior groundbreaking ADC designs from imec, cleverly exploiting the opportunities of modern advanced CMOS technologies. Scaling toward smaller technology nodes will result in an even better performance of the ADC."

Provided by IMEC

Citation: Record ADC for next-generation software defined radio (2014, June 11) retrieved 26 April 2024 from <https://phys.org/news/2014-06-adc-next-generation-software-radio.html>

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