Research promises to lead to increased functionality for advanced mobile devices

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University of California, Berkeley researchers sponsored by Semiconductor Research Corporation, are pursuing a novel approach to 3D device integration that promises to lead to advanced mobile devices and wearable electronics featuring increased functionality in more low-profile packages.

The research focuses on integrating extra layers of transistors on a vertically integrated 3D monolithic chip using printing of semiconductor "inks" as compared to the current method of chip-stacking through 3D interconnect solutions.

The new process technology could help semiconductor manufacturers develop smaller and more versatile components that are less expensive and higher performing by enabling cost-effective integration of additional capabilities such as processing, memory, sensing and display. The low-temperature process is also compatible with polymer substrates, enabling potential new applications in wearable electronics and packaging.

Current efforts on 3D integration have used transfer of thin single crystal semiconductor layers, polycrystalline silicon deposited by chemical vapor disposition, or other growth techniques to realize integrated devices.

"Compared to these approaches, we believe our approach is simpler and potentially with significantly lower cost," said Vivek Subramanian,

professor of Electrical Engineering and Computer Sciences at UC Berkeley. "Our goal in this work is to maximize performance, with the hope that this will make the cost versus performance tradeoff worthwhile relative to other approaches."

Specifically, the UC Berkeley team is developing directly-printed transparent oxide transistors as a path to realizing additional layers of active devices on top of CMOS metallization.

To fabricate such devices, new material and process methodologies are needed for depositing nanoparticles for semiconductors, dielectrics and conductors. The research is particularly focused on solution-based processing due its low temperature compatibility with CMOS metallization as well as the potential for lower cost manufacturing.

"Initial results from the Berkeley team show that reasonably high performance can be obtained from ink-jet printed devices with process temperatures that are compatible with post-CMOS metallization, thus enabling a new route to monolithic 3D integration," said Bob Havemann, Director of Nanomanufacturing Sciences at the SRC.

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