Toshiba's low leakage SRAM enables fast wake-up from a deep sleep mode

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Toshiba Corporation today announced that it has developed an eXtremely Low Leakage 65nm SRAM (XLL SRAM) suitable for back-up RAM in low power MCU that achieves a fast wake-up time from a deep sleep mode.

Toshiba presented this development at the 2014 IEEE International Solid-State Circuits Conference in San Francisco, California, on February 11.

There is strong demand for long battery discharge times in low power systems, including wearable devices, healthcare tools and smart meter. Although there are many challenges to reduce power of MCU used in these systems, with advances in the process generation, increasing of leakage current becomes problem as well as active power consumption. Reducing leakage current in RAM, which retains data during stand-by, is particularly important.

A typical MCU reduces power dissipation with a deep sleep mode, where stand-by current is under 1µA. However, this makes it impossible for typical SRAM to retain data, as SRAM require a stand-by current much higher than 1µA. As a result, data reloading takes a long time when the system wakes up from a deep-sleep mode. Use of FRAM as back-up RAM eliminates this reload problem, but FRAM is much slower and consumes more active power than SRAM and also needs more process cost.

Toshiba has developed an eXtremely Low Leakage SRAM (XLL

SRAM) that has a leakage rate a thousand times lower than that of conventional SRAM; 27fA leakage current per bit when fabricated in 65nm process. This level is lower than that found in published data for SRAM beyond 65nm technology. The new SRAM can retain data for over 10 years with a single battery charge, in a back-up memory with a capacity of around 100Kbyte.

MOSFET fabricated with recent process technology has higher gate leakage, gate induced drain leakage (GIDL) and channel leakage. Toshiba has developed a low leakage transistor with thick gate oxide, long channel length and optimum source drain diffusion profile to reduce these leakage factors, and adopt it in the SRAM memory cell. The company has developed several innovative leakage reduction circuits. One is a source bias circuit to apply reverse back-bias to NMOS of memory cell, and another cuts off the supply voltage to peripheral circuits during data retention.

The low leakage transistor is larger than conventional transistor, increasing the overall cell area. Toshiba secured a 20% reduction in cell size compared to area designed by original design rule of this device under the condition of 1.2V supply voltage. Generally, large transistor circuits have higher active power dissipation. Toshiba has suppressed this by adopting "Quarter Array Activation Scheme (QAAS)" and "Charge Shared Hierarchical BitLine (CSHBL)" power reduction circuits.

An SRAM with a 7ns read access time is fast enough to be used as working RAM in low power MCU and for use as back-up RAM in deep-sleep mode because of its extremely low leakage current. As the system eliminates data reloading, the wake-up time from deep sleep mode is boosted.

Toshiba plans to use the SRAM in a product released in 2014, and

expects to see wide use in coming battery-driven products.

Provided by Toshiba

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