Scientist developing 3-D chips to expand capacity of microprocessors

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(Phys.org) —Many researchers in the field of integrated circuits worry that the fast paced progress of "miniaturization" will start to slow unless they find new ways to expand the capacity of the conventional two-dimensional chips used today in virtually all electronics.

Emre Salman, an assistant professor of computer and electrical engineering at Stony Brook University, is trying to design new technology, circuits and algorithms for the next generation of microprocessors, mobile computing devices and communication chips, in order "to overcome the fundamental limitations of current electronic systems, such as high power consumption," he says.

Specifically, the National Science Foundation (NSF)-funded scientist is working on developing three-dimensional integration, an emerging technology that would vertically stack multiple wafers, a technique with the potential to enhance significantly the capability of the current two-dimensional chips.

"Today's typical electronic system on a circuit board consists of multiple chips connected with wires that are at the millimeter and centimeter scale," he explains. "These bulky connections not only slow down the circuit, but also consume power and reduce the reliability of the system."

In 3-D integration technology, on the other hand, those discrete chips, now called tiers, are stacked on top of each other before they are packaged, he says. "The entire 3-D system is placed in a single package,"

he says. "Vertical connections that achieve communication among the tiers are now in the micrometer scale, and getting even shorter with advances in 3-D manufacturing technology, thereby consuming less power and providing more performance. Essentially, 3-D technology enables higher and heterogeneous integration at a smaller form factor."

This goal, however, faces any number of challenges. "This expansion comes with a variety of difficulties," says Salman, who also directs Stony Brook's Nanoscale Circuits and Systems (NanoCAS) Laboratory. "For example, it is highly challenging to ensure that the diverse planes of a 3-D chip work in harmony as a single entity."

He points out that many scientists have been working on wafer level 3-D integration for more than a decade. However, "the primary emphasis has been on high performance and somewhat homogeneous chips, such as microprocessors," he says.

On the other hand, citing the 2011 edition of the International Technology Roadmap for Semiconductors (ITRS), an important guide for researchers in the field, "the third phase and long term application of 3-D technology includes highly heterogeneous integration, where sensing and communication planes are stacked with conventional data processing and memory planes," he says.

This means that a single 3-D chip will be able detect data from environment, then process and store this data using advanced algorithms, and then wirelessly transmit these data to a remote center, he says.

Unlike the dominant existing research, this relatively long term application has become his team's primary focus, an approach with the potential to enlarge the three-dimensional domain from high performance computing to relatively low power systems-on-chip (SoCs). These low power SoCs have capabilities beyond the boundaries of

traditional general purpose processors, since they integrate multiple functions, including sensing, processing, storage and communication into a single 3-D chip, he says.

"Numerous applications exist in health care, energy efficient mobile computing, and environmental control, since a smaller form factor can be achieved at lower power while offering significant computing resources," he says. "Our fundamental objective is to develop a reliable 3-D analysis and design platform for these applications which will host future electronics systems that are increasingly more portable, can interact with the environment, consume low power, yet still offer significant computing capability."

He is conducting his research under an NSF Faculty Early Career Development (CAREER) award. The award supports junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education and the integration of education and research within the context of the mission of their organization. NSF is funding his work with $453,809 over five years.

"We are developing design methodologies to reliably distribute power to each tier of a 3-D chip," he says. "We are also exploring novel circuit topologies for 3-D power management, thereby increasing energy efficiency. We are investigating various noise coupling paths within a 3-D system, and finding ways to protect sensitive transistors from noise. All of these activities serve for the common goal of improving power, signal and sensing integrity of a heterogeneous 3-D chip."

At the NanoCAS lab, their workstations are equipped with the latest electronic design automation software that allows the researchers to verify their algorithms, models and design methodologies. "We primarily rely on these state-of-the-art IC simulation tools that the semiconductor industry uses to design and verify their chips," he says.

As part of the grant's educational component, Salman plans to integrate these research activities at the secondary, undergraduate and graduate levels, and will involve the NanoCAS lab in an engineering summer camp for high-school students organized at Stony Brook. The program, organized jointly by the department of electrical and computer engineering and the student branch of IEEE (the Institute of Electrical and Electronics Engineers, a world-wide professional association) at Stony Brook, consists of a two-week residential camp at the university campus.

"While the primary goal is to introduce motivated high school students to the field of electrical engineering through theoretical classes and hands-on projects, the students also have an opportunity to learn and experience the university campus life," Salman says.

"At the NanoCAS lab, we offer an experimental course on fiber optic communication," he adds. "The course starts with an interesting history of communication technologies from prehistoric times to modern day. The students then learn the fundamentals of optical voice link and design their own communication link by soldering electronic components. We believe that an efficient link between education and research is essential for the advancement of science and technology to prevail."

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