

# Imec demonstrates strained germanium finFETs at IEDM 2013

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At this week's IEEE International Electron Devices Meeting (IEDM 2013), imec reported the first functional strained germanium (Ge) quantum-well channel pMOS FinFETs, fabricated with a Si Fin replacement process on 300mm Si wafers. The device shows a possible evolution of the FinFET/trigate architecture for 7nm and 5nm CMOS technologies.

Since the 90nm technology, embedded SiGe source/drain has been a popular stressor method to produce strained Si that enhances pMOS devices. With diminishing [device](#) dimensions, the volume to implement stressors in the source and drain has also been severely scaled. Especially, with thin-body devices like FinFETs, the difficulty is even more pronounced. A possible relief would be to implement highly-strained material directly into the channel itself.

Imec's solution, growing compressively strained Ge-channels on relaxed SiGe buffer, has already proven to boost the channel mobility, and is also known for its excellent scalability potential. The use of a fin replacement process to fabricate the strained Ge channel device makes it especially attractive for co-integration with other devices on a common Silicon substrate. The reported strained Ge p-channel FinFETs on SiGe trench buffer achieved peak transconductance ( $gm_{SAT}$ ) values of  $1.3\text{mS}/\mu\text{m}$  at  $V_{DS}=-0.5\text{V}$  with good short channel control down to 60nm gate length. The transconductance to subthreshold slope ratio of the devices ( $gm_{SAT}/SS_{SAT}$ ) is high compared to published relaxed Ge FinFET devices.

Future developments will focus on improving the device performance through P-doping in the SiGe, optimizing Si cap passivation thickness on the Ge, and improving the gate wrap of the channel. "Unlike published Ge FinFETs, this work demonstrates a Ge-SiGe heterostructure-based quantum-well device in a FinFET form, which not only provides strain benefits but also enhances short-channel control," remarked Nadine Collaert, program manager of the Ge/III-V device R&D.

"Just recently, we reported the implementation of III-V material into the device architecture using a fin replacement process," stated Aaron Thean, director of the logic R&D program at imec. "This new achievement, implementing Ge into the [channel](#) through our fin replacement process, is another key ingredient to our menu of process possibilities for monolithic heterogeneous integration to extend CMOS and SOCs."

Provided by IMEC

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