Fujitsu semiconductor introduces innovative methodology for leading-edge "Customized soC" design

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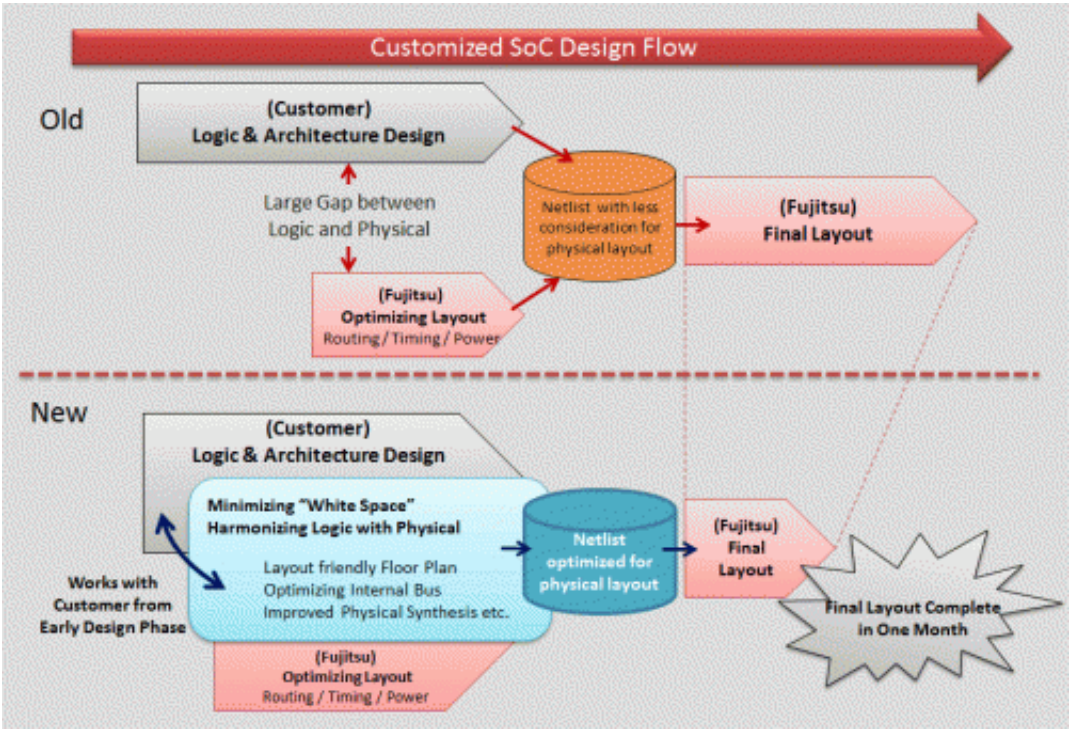

Fig1. Overview of New Methodology

Fujitsu Semiconductor today announced that it has developed a new design methodology that enables both the higher circuit density and the shorter development time, for advanced 28nm SoC (System on a Chip) devices. Incorporating the new methods can improve the circuit density by 33%, and reduce the time for final layout process to as short as one

month. It will be integrated into the company's new Customized SoC Solutions, and will be available for the development of RTL-handoff SoCs for customers. Fujitsu will start accepting orders to develop SoCs using the new methodology in February 2014.

SoCs with the leading-edge technology, such as 28nm process, are required to have more and more functionality and performance, which drive the need for more circuits packed into the chip. Designing such SoCs is becoming increasingly complex and taking significantly longer development time, while addressing the power consumption is also becoming more challenging. In order to cope with such difficult SoC design, Fujitsu semiconductor has developed innovative design methods that enable higher density, shorter development time, and lower power consumption.

New design method to minimize "White Space"

- New proprietary procedures have been implemented for estimating more layout-friendly floor plans, as well as for considering wiring routs and timing closure to optimize internal data buses. These steps will help minimize the "white space" in which no transistors are placed, and thus allow more circuits to fit in a chip.

Proprietary technology for harmonizing the logic with the physical architecture

- It automatically synthesizes the net list data for physical layout, without the need to manually change the logic design. This will bring improved routability and ease of timing closure, resulting in less time required for final layout process, as well as even higher density integration.

Compared with the conventional design, implementing these new methods will allow designers to add 33% more circuits in a die of the same size, and the final layout process can be completed in as short as one month.

The new methodology will be integrated into Fujitsu Semiconductor's Customized SoC Solutions, and will be available for the development of RTL-handoff SoCs. It will start accepting the order in February 2014.

Leveraging the track record and expertise as a world-class ASIC vendor over many years, Fujitsu Semiconductor is providing one-stop Customized SoC Solutions that integrate advanced design implementation, manufacturing , and services like system-level study and development assistance. Through the offering of these solutions, Fujitsu Semiconductor supports the rapid development of high-performance and energy efficient SoC devices for its customers.

Provided by Fujitsu