

Cost-saving computer chips get smaller than ever

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Not so long ago, a computer filled a whole room and radio receivers were as big as washing machines. In recent decades, electronic devices have shrunk considerably in size and this trend is expected to continue,

leading to enormous cost and energy savings, as well as increasing speed.

Key to shrinking devices is Terascale computing, involving ultrafast technology supported by single microchips that can perform trillions of operations per second.

Using Terascale technology, [semiconductor components](#) commonly used to make [integrated circuits](#) for all kinds of appliances could measure less than 10 nanometres within several years. Keeping in mind that a nanometre is less than 1 billionth of a metre, electronic devices have the potential to become phenomenally smaller and require significantly less energy than today - a development that will revolutionise the electronics industry.

Despite progress, the technology for producing these ultra-small devices has a long way to go before being reliable. To advance the work, the EU-funded project TRAMS ('Terascale reliable adaptive [memory systems](#)') sought to improve reliability by improving [chip design](#).

The TRAMS team conducted in-depth variability and reliability analyses to develop chip circuits that are much less prone to errors. These circuits feature new designs that yield reliable memory systems from currently unreliable nanodevices.

The main challenge was to develop reliable, energy efficient and cost effective computing using a variety of new technologies with individual transistors potentially measuring below five nanometres in size.

The team investigated a number of technologies and materials with potential to make Terascale computing a reality. These included:

- carbon nanotubes (very tiny cylindrical [nanostructures](#) grapheme technology);

- new transistor geometries, such as FinFETs;
- state-of-the-art [nanowires](#), which offer very advanced transistor capabilities for use in a new generation of electronic devices.

Using models, the researchers analysed reliability - from the technology to the circuit level.

These advances are expected to redefine today's standard 'complementary metal-oxide semiconductors' (CMOS). The team's results would help Europe's manufacturers develop CMOS devices below the 16 [nanometre](#) range. The biggest challenge will lie in reducing CMOS devices to below five nanometres - a development that now starts to look possible.

From communication and security to transport and industry, CMOS-based devices of the future promise to redesign the technology we use, introducing radical energy and cost savings.

The TRAMS consortium includes universities and companies from Spain, Belgium and the UK. The project was coordinated by Spain's Universitat Politècnica de Catalunya, and received almost EUR 2.5 million in EU funding. The team concluded its work in December 2012.

More information: TRAMS trams-project.upc.edu/

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