

# NIST chip measurement advance earns 'oscar of innovation'

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A fundamental advance in measurement capabilities that could save semiconductor manufacturers billions of dollars annually has earned a 2013 R&D 100 Award for its National Institute of Standards and Technology (NIST) inventors.

Called quantitative hybrid metrology (QHM), the new NIST method integrates statistical techniques and measurements made with two or more instruments to rigorously determine the sizes of nanoscale transistor features on semiconductor chips. In one demonstration the final measurement was three times more accurate than the results achieved with any one method alone.

The NIST inventors of QHM include physicists Bryan Barnes and Richard Silver and statistician Nien Fan Zhang. Hui Zhou, a NIST research associate, was a member of the development team.

On the basis of a 2007 paper, the team estimates that a three-fold decrease in measurement uncertainty achievable with their innovation could save manufacturers as much as \$7 for each chip they produce.

The public-domain invention does not replace chip makers' standard measurement tools, such as scanning electron microscopes (SEMs) and optical devices known as scatterometers. Rather, the new method enhances these tools and ties them together in novel combinations. This flexibility in measurement strategies minimizes measurement uncertainties and optimizes throughput.

A key element of the NIST method is a model library—a collection of simulated data based on typical chip feature dimensions that are compared to actual measurements, made with an SEM, scatterometer, or by other means.

Before performing the comparison, however, the NIST team employs an elegant statistical treatment—called Bayesian analysis—to incorporate a few key additional measured values from other tools into the library model. This step reduces the uncertainty in the measurements, lowering them by more than a factor of three in some cases.

Several companies and other organizations, including IBM, GlobalFoundries, the University of California Berkeley and Sematech are adopting hybrid metrology. All have made important advances in their implementations of the technique since the inventors first introduced the statistical foundations to quantitative hybrid metrology.

Beyond immediate applications, QHM has the potential to be a cost-effective solution to an imposing challenge facing high-volume [semiconductor manufacturers](#) as dimensions decrease below 20 nanometers (nm). By 2019, transistor dimensions are slated to shrink to 10.9 nm. At present there are no known solutions for measuring critical dimensions of that scale on chips, according to the International Technology Roadmap for Semiconductors.

"No single measurement technique can fulfill this critical need that is central to the continued success of the entire semiconductor industry," according to the inventors. "Measurement-tool combination through QHM is uniquely positioned as the best option for process control for circuits with line widths below 10 nm."

To foster the adoption of this technology among semiconductor manufacturers and to facilitate collaboration among measurement

instrument makers, this novel technology was placed in the public domain.

For more, see [phys.org/news/2012-09-refined-...n-accuracy-chip.html](https://phys.org/news/2012-09-refined-...n-accuracy-chip.html)

**More information:** N.F. Zhang, R.M. Silver, H. Zhou and B.M. Barnes. Improving optical measurement uncertainty with combined multitool metrology using a Bayesian approach. *Applied Optics*, Vol. 51, No. 25. Sept. 1, 2012. DOI: [dx.doi.org/10.1364/AO.51.006196](https://dx.doi.org/10.1364/AO.51.006196).

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