Taking transistors into a new dimension

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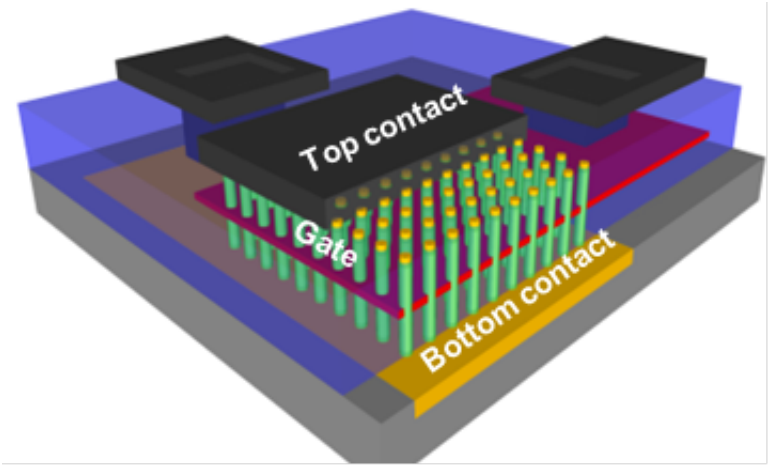

Diagram of a 3D nano-transistor showing the gate (red) surrounding the vertical nanowires (green) and separating the contacts at the ends of each nanowire (beige). Credit: © X-L Han and G. Larrieu

A new breakthrough could push the limits of the miniaturization of electronic components further than previously thought possible. A team at the Laboratoire d'Analyse et d'Architecture des Systèmes (LAAS) and Institut d'Électronique, de Microélectronique et de Nanotechnologie (IEMN) has built a nanometric transistor that displays exceptional properties for a device of its size. To achieve this result, the researchers developed a novel three-dimensional architecture consisting of a vertical nanowire array whose conductivity is controlled by a gate measuring only 14 nm in length.

Published in *Nanoscale*, these findings open the way toward alternatives

to the planar structures used in microprocessors and memory units. The use of 3D transistors could significantly increase the power of microelectronic devices.

The "building blocks" of microelectronics, transistors consist of a semiconductor component, called channel, linking two terminals. The flow of current between these terminals is controlled by a third terminal, called gate. Acting like a switch, the gate determines whether the transistor is on or off. Over the past 50 years, transistors have been steadily reduced in size, enabling the development of increasingly powerful microelectronic devices. However, it is generally agreed that today's transistors, with their planar architecture, are nearing the limits of miniaturization: there is a minimum size under which the gate control over the channel becomes less and less effective. In particular, leakage currents begin to interfere with the logical operations performed by the transistor array. To overcome this problem, researchers around the world are investigating alternatives that will allow the race for miniaturization to continue.

A team of researchers at the LAAS and IEMN has now built the first truly three-dimensional nanometric transistor. The device consists of a tight vertical nanowire array of about 200 nm in length linking two conductive surfaces. A chromium gate completely surrounds each nanowire and controls the flow of current, resulting in optimum transistor control for a system of this size. The gate is only 14 nm in length, compared with 28 nm for the transistors in today's chips, but its capacity to control the current in the transistor's channel meets the requirements of contemporary microelectronics.

This architecture could lead to the development of microprocessors in which the transistors are stacked together. The number of transistors in a given space could thus be increased considerably, along with the performance capacity of microprocessors and memory units. Another

significant advantage of these components is that they are relatively simple to manufacture and do not require high-resolution lithography. In addition, these 3D transistors could be easily integrated into the conventional microelectronic devices used by the industry today.

A patent has been filed for these transistors. The researchers now plan to continue their efforts to further reduce the size of the gate, which they believe could be made smaller than 10 nm while still providing satisfactory control over the transistor. In addition, the team is looking for industrial partners to help design the electronic devices of the future using the 3D architecture of these novel transistors.

More information: Vertical nanowire array-based field effect transistors for ultimate scaling.. G. Larrieu and X.-L. Han. *Nanoscale*, online as of 23 January 2013 doi:10.1039/C3NR33738C

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