

Researchers utilize atomic layer etch analysis to accelerate development of green chemistries

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Researchers sponsored by Semiconductor Research Corporation (SRC) today announced development of a modeling process designed to simulate atomic-level etching with chemicals that are effective alternatives to widely used perfluorocarbon (PFC) gases. The novel approach under way at the University of California, Los Angeles (UCLA) will identify and evaluate green plasma chemistries for processing emerging memory/logic devices and through-silicon-via (TSV)-enabled technologies for the semiconductor industry.

In order to continue the advancement of transistor and [memory cell](#) performance, the research will focus on several promising new materials that have been introduced for [future generations](#) of [integrated circuits](#) (ICs). To exploit this opportunity, the industry requires new and effective etch processes with which to pattern the next-generation fabrics.

The aim of the UCLA research effort within the SRC-funded Engineering Research Center for Environmentally Benign Semiconductor Manufacturing (ERC) is to identify environmentally friendly chemistry for patterning materials in IC fabrication and verify their performance to be equal to, or greater than, current state-of-art plasma chemistries.

The unique performance characteristics required for advanced devices

and technologies dictates the use of certain materials and corresponding aggressive etch chemistries. Next-generation processes will benefit from chemicals that are more benign, less hazardous and more efficiently utilized.

The advanced modeling approach developed by UCLA will predict emissions from plasma processes and assess the effectiveness of non-PFC etch chemistries compared to those using PFC gases. While historically PFC gases have been an enabling component of semiconductor manufacturing, the industry continues to aggressively pursue and implement PFC replacement and abatement strategies. The UCLA research will greatly assist and accelerate this industry effort.

"The industry can't afford to conduct thousands of hands-on experiments to measure, one at a time, the chemical reactions that etch at a molecular scale," said Dr. Jane Chang, lead researcher for the SRC-funded activity at UCLA. "With modeling, we can conduct those evaluations in a relatively short time. In terms of months rather than years, we expect to identify the conditions for a benign etch chemistry that will help to facilitate the industry's technology roadmaps."

Peeling Layers at the Atomic Level

Chemical vapor deposition and plasma etch have been extensively used as part of an integrated process flow to realize chip manufacturing over the last several decades.

In this era of nanotechnology, atomic layer deposition has become a viable approach to synthesize functional materials for chip manufacturing. However, its counterpart, atomic layer etch, has not been fully developed.

The UCLA program is designed to reverse engineer the atomic layer

deposition process, providing guidance for simulation of the atomic-layer etch. Such capability is projected by industry scientists to become increasingly important in order to achieve the patterning of complex and multi-layer thin-film structures.

For example, new composite or hybrid materials required for emerging memory and [logic devices](#) pose significant etch challenges that must be addressed by aggressive, yet highly selective, etch chemistries.

Conversely, PFC replacement etches for TSVs, which enable 3D device integration, face a different set of challenges such as high aspect ratio and multiple interfaces. Both types of etching present difficult challenges, but also significant opportunities to enable higher density, performance and functional diversification in future ICs.

By screening potential surface reactions and applying thermodynamic and kinetics assessment to measure reaction, researchers are taking a unique approach to remove specific surface elements and design chemistries that will work better than PFCs. As a result, the model prediction provides a design of experiments that can be much more efficient and shorten the timeframe for discovery and confirmation of alternative chemicals.

"Atom by atom, this is the fastest and most affordable way to discover the best approaches for etching down to silicon and metal layers with a variety of chemicals for chipmaking," said Farhang Shadman, Director of the SRC-funded ERC based at the University of Arizona.

Next Steps

According to the World Semiconductor Council, semiconductor manufacturers in the European Union, Japan, Korea, Taiwan and the United States voluntarily lowered PFC emissions by more than 30 percent between 1995 and 2010, surpassing the WSC goal to reduce

emissions by 10 percent. UCLA predicts that its modeling approach will lead to further reductions in PFC emissions from semiconductor manufacturing, supporting the industry's ongoing commitment to environmental protection.

An additional potential benefit of the UCLA atomic scale etch model is an improvement in throughput for chip production by identifying and confirming higher etch-rate processes.

"Needless to say, accelerating the pace of PFC replacement is an important priority for the [semiconductor industry](#), and SRC member companies are working closely with Dr. Chang's UCLA research team to provide both guidance and support in developing and verifying these new models," said Bob Havemann, Director of Nanomanufacturing Sciences at SRC. "This project provides an outstanding example of the vital ongoing research at the ERC, which is focused on developing ESH-preferable processes for current and future [semiconductor manufacturing](#)."

Provided by Semiconductor Research Corporation

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