Analog to digital converter research improves Internet speeds to 100 Gb/second

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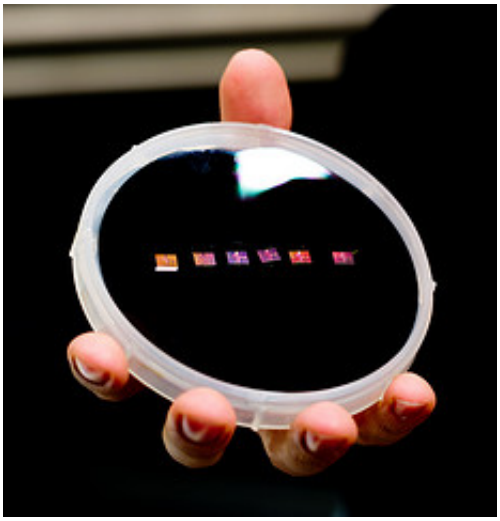

(Phys.org)—Scientists from IBM Research and Ecole Polytechnique Fédérale de Lausanne (EPFL) in Switzerland unveiled a technological achievement in signal conversion technology that can improve Internet speeds to 100 Gigabits per second (Gb/s), doubling current technology on the market today. The research was presented at the International Solid-State Circuits Conference (ISSCC) on February 20.

The annual growth rate of structured and unstructured Big Data is 60 percent. A large portion of this is real world data from the environment, including images, light, sound and even the radio signals from the Big

Bang 13 billion years ago—and it's all analog.

To make use of this data in computers the analog signal needs to be converted to digital, in the form of zeros and ones. This is done using an analog to digital converter or ADC, which approximates the right combination of zeros and ones to digitally create the data. For example, the sound of automobiles driving on a highway may be represented as "0010011000110100".

With the rapid growth of Big Data and the Internet of Things, several years ago IBM scientists began developing energy efficient ADCs to bring large numbers of real world analog signals on logic chips for computation.

"Most of the ADCs on the market today weren't designed to handle the massive Big Data applications we are dealing with today—it's the equivalent of funneling water through a straw from a fire hose," explains Dr. Martin Schmatz, Systems department manager at IBM Research. "This is IBM's first attempt at designing a new ADC that leverages a standard CMOS logic process, not only resulting in the most efficient ADC in its class, but also opening the possibility to add massive computation power for signal analysis on the same chip with the ADC."

The ADC design has been developed at IBM Research in Zurich, in collaboration with scientists of the Microelectronic Systems Laboratory of EPFL. "The new ADC design has several key advantages over similar designs proposed earlier: in terms of speed, power dissipation, and silicon area" says Professor Yusuf Leblebici, director of the Microelectronic Systems Laboratory. "It is a perfect example of successful industry-university cooperation, having produced world-class results."

The prototype ADC was manufactured at IBM's 300 mm fab in East

Fishkill, NY in a 32 nanometer silicon-on-insulator CMOS process with a tiny core area of 22×70 μm^2. The ADC generates one billion analog-to-digital conversions per second operating from a single 1 V supply, with a total power consumption of 3.1 mW—approximately 30 times less than what a cellphone uses when it's idle.

For its speed and efficiency the resolution of 8 bits is also within the limits for many applications ranging from supercomputers and data centers to consumer applications, including cable modems, set-top boxes and mobile devices—the average smartphone can have more than 10 ADCs for example in temperature, touch screen and motion sensors.

IBM scientists are also considering the ADC to help convert analog signals that originate from the Big Bang. The project is called DOME and it's a collaboration between ASTRON, the Netherlands Institute for Radio Astronomy, and IBM to develop a fundamental IT roadmap for the Square Kilometer Array (SKA), an international project to build the world's largest and most sensitive radio telescope.

The analog data that the SKA collects from deep space is expected to produce 10 times the global internet traffic and the IBM prototype ADC would be an ideal candidate to convert the analog data to digital at very low power—a critical requirement considering the thousands of antennas which will be spread over 3,000 kilometers (1,900 miles).

The ADC could be available as early as 2014.

The scientific paper is entitled, "A 3.1 mW 8b 1.2 GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32 nm Digital SOI CMOS".

Provided by IBM