Toshiba's low-power SRAM chip aims to cut device drain

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(Phys.org)—Toshiba has announced a low-power embedded SRAM memory chip which may make future mobile devices last longer. Presenting its SRAM developments at the International Solid-State Circuit Conference in San Francisco in February, Toshiba said that its low-power design technique could help cut active and standby power consumption by 27 percent and 85 percent, respectively. Toshiba accomplished this by using a bit-line power calculator, or BLPC, to predict the power consumption of the bit lines and to monitor consumption of SRAM rest circuits, and a digitally-controllable retention circuit, or DCRC.

The DCRC is used to decrease standby power by updating the size of the buffer in the retention driver.

Toshiba noted its technology advancement is suited for smartphones and other mobile products. The technology reduces active and standby power in temperatures ranging from room temperature to high temperature through use of this BLPC and DCRC.

Tokyo-based Toshiba further noted that "longer battery life requires lower power consumption in both high performance and low performance modes (MP3 decoding, background processing, etc.). As low performance applications require only tens of MHz operation, SRAM temperature remains around RT, where active and leakage power consumptions are comparable. Given this, the key issue is to reduce active and standby power from HT to RT."

More information: www.semicon.toshiba.co.jp/eng/ … pics_130222_e_1.html