Highly energy-efficient CMOS logic systems

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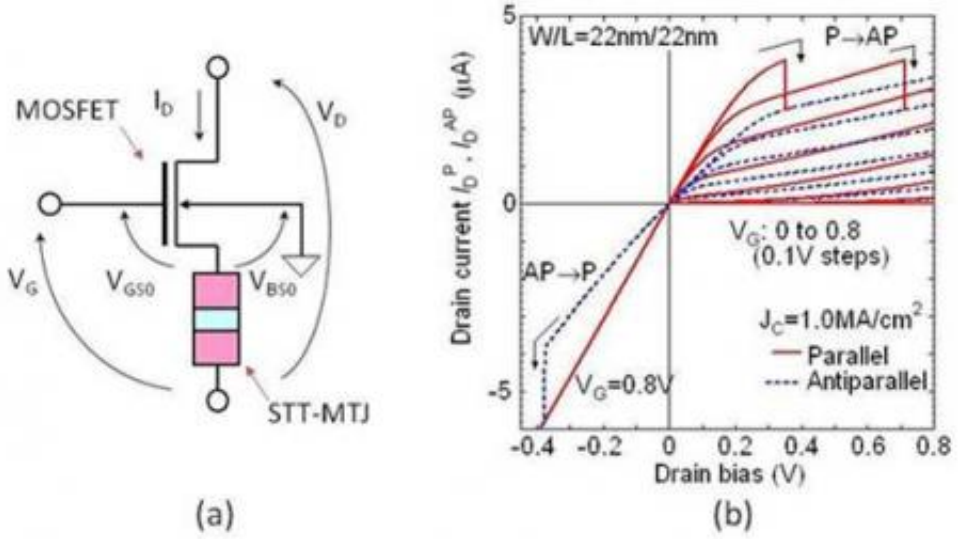

(a) Circuit configuration of PS-MOSFET, in which the STT-MTJ connected to the source of the MOSFET feeds back its voltage drop to the gate, and the degree of negative feedback depends on the resistance state of the STT-MTJ.(b) Simulated output characteristics and current-induced magnetization swiching (CIMS) behavior of the PS-MOSFET.

Non-volatile bistable memory circuits being developed by Satoshi Sugahara and his team at Tokyo Tech pave the way for highly energy-efficient CMOS logic systems. The details are described in the February 2013 issue of *Tokyo Institute of Technology Bulletin*.

Developments in low power, high performance CMOS logic technology are vital to the future of microprocessors and system-on-chip (SoC) devices for personal computers, servers, and mobile/smart phones. Much of the processing in these computing systems is carried out using a volatile hierarchical memory system in which bistable circuits such as static random access memory (SRAM) and flip-flop (FF) play an essential role for fast data-access. However, the power to these bistable circuits cannot be switched off without losing their data. This inability to turn off power is a fundamental problem for energy consumption in CMOS logic systems.

The method for saving energy in CMOS logic systems, called power-gating, uses architecture to cut the supply voltage to idle circuit domains, effectively putting them to power shut-off state to avoid leakage and thereby save static energy. Satoshi Sugahara and his team at the Tokyo Institute of Technology have proposed a new architecture of power-gating using non-volatile SRAM (NV-SRAM) and non-volatile FF (NV-FF) circuits, called non-volatile power-gating, so that the size of logic circuit domains for power-gating is optimally designed, supply voltages to the domains are cut at the optimum times, and the energy cost of the logic circuits is worthwhile.

Over the past few years, Sugahara and his team have been developing non-volatile bistable memory circuits (NV-SRAM and NV-FF) required to establish non-volatile power-gating systems with better overall performance and energy efficiency than conventional power-gating systems. In particular, the researchers have built pseudo-spin metal–oxide–semiconductor field-effect transistors (PS-MOSFETs) for use in the non-volatile bistable memory circuits.

The PS-MOSFET can be configured with an ordinary MOSFET coupled with a spin-transfer torque magnetic tunnel junction (STT-MTJ), and it can reproduce the functions of spin-transistors – in which different

electrons spin states or magnetization configurations of the ferromagnetic electrodes are used to control transistor output1. Spin transistors can also store non-volatile information1. In a typical bistable memory circuit, an inverter loop consisting of cross-coupling two CMOS gates is used to store each memory bit. In the new non-volatile bistable circuits, PS-MOSFETs are added to the inverter loop.

Previous attempts to build non-volatile bistable circuits with STT-MTJs have resulted in performance degradation, because the STT-MTJs interfere with their fundamental circuits of the inverter loops. To overcome this problem, the team designed NV-SRAM and NV-FF circuits using PS-MOSFETs. In these circuits, the STT-MTJs can be electrically separated from the inverter loops by the PS-MOSFETs and thus have no degradation effects on the bistable circuit performance.

The NV-SRAM and NV-FF circuits built by Sugahara's team have performed well under tests so far, compared to conventional SRAM/FF circuits. They also developed architectures for minimizing break-even time (that is an important performance index of power-gating) of the NV-SRAM and NV-FF circuits, including a 'store-free' shutdown, wherein existing data is not rewritten, thereby dramatically saving energy.

These new transistor and circuit designs could be pivotal in the development of faster, more energy-efficient processing in future CMOS logic systems. Most importantly, as the researchers state in a recent publication2-5, "Proposed architectures have excellent compatibility with present microprocessor/SoC technologies", and "Proposed non-volatile bistable circuits using PS-MOSFETs can dramatically reduce the energy issues caused by static power dissipation in advanced CMOS logic systems".

More information: Sugahara, S. , Nitta, J. Spin-Transistor Electronics: An Overview and Outlook, *Proceedings of the IEEE*, vol.98, no. 12,

2010, pp. 2124-2154. www.titech.ac.jp/bulletin/arch … y/topics/vol291.html

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