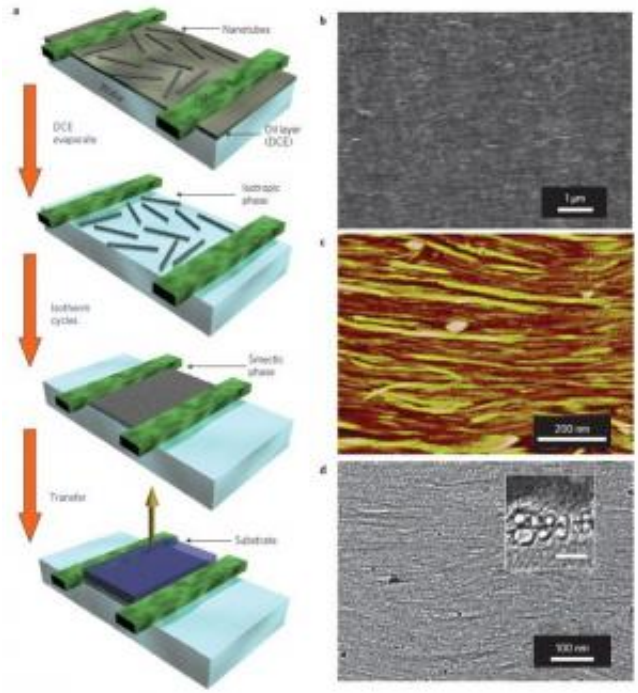
Densest array of carbon nanotubes paves way toward post-silicon technology

February 14 2013, by Lisa Zyga



(a) The assembly of a dense, full-coverage nanotube array, and (b) microscopic images of the aligned nanotubes. The study takes carbon nanotubes a step closer to replacing silicon in electronic devices. Image caption: Qing Cao, et al. ©2013 Macmillan Publishers Limited

(Phys.org)—Single-walled carbon nanotubes may one day replace the silicon in electronics, but in order to do so, the nanotubes must be aligned in dense arrays for optimal performance. So far, the highest nanotube density is less than 50 tubes/μm, but in a new study researchers

have broken this record by achieving a density of more than 500 tubes/μm. The higher density leads to better performance, bringing nanotubes a step closer to playing a role in post-silicon technologies.

The researchers, Qing Cao at the IBM T.J. Watson Research Center in Yorktown Heights, New York, and coauthors, have published their study on the dense arrays of carbon nanotubes in a recent issue of *Nature Nanotechnology*.

As the researchers explained, carbon nanotube-based electronics with the best electrical properties should have nanotubes that are purely semiconducting, that are well-aligned, and that form arrays with a density as high as possible, up to covering the entire substrate.

To meet these requirements, the researchers used a fabrication technique called the Langmuir-Schaefer method, which involves dispersing pre-enriched semiconducting nanotubes on a water surface. The floating nanotubes spread out to cover the whole surface as a result of the surface tension. Applying a compressive force assembles the nanotubes into well-ordered arrays, and the compression is stopped when the nanotube film becomes incompressible, which indicates that nanotube arrays have covered the entire surface. The resulting nanotube arrays have a 99% semiconducting purity and are aligned within 17° of one another.

As the researchers explain, the biggest improvement comes from the increased density. Whereas previous arrays with densities of less than 50 tubes/μm density cover about 10% of a surface, the new array with 500 tubes/μm density can cover almost 100% of a surface. Images from a tunneling electron microscope further reveal that a surface with nanotubes packed in a double layer has an estimated tube density as high as 1,100 tubes/μm.

The increased density provides substantial improvements in the

properties of electronic devices built with nanotubes. For example, low-cost thin-film electronics could be built on carbon nanotubes and realize novel applications such as economically disposable, mechanically flexible, and/or optically transparent electronic devices. Most carbon nanotube thin-film transistors reported so far have been constructed with array or network densities of 6-10 tubes/μm. This limited surface coverage results in a gate capacitance per area that is about 10 times lower than that of conventional thin-film transistors built on materials like amorphous silicon or oxide semiconductors, which decreases the operating speed and increases the output resistance. On the other hand, transistors built with the high-density nanotube arrays can completely overcome this limitation, leading to a significantly improved device performance.

Researchers also expect carbon nanotubes to replace silicon at the end of the current scaling roadmap to further extend Moore's law. For such high-performance applications, high tube density is required to achieve high current output density, which allows faster operating speed and higher device packing density. Compared to the previous best results obtained on devices constructed with an array density of 4 tubes/μm, scaled nano-transistors built with the high-density arrays demonstrate several times better performance, with the highest transconductance and current density reported yet for nanotube transistors together with a high on/off ratio about 10^3.

The researchers here predict that the electrical properties of the high-density nanotube arrays can be further improved by making several modifications, such as improving the electrical contact between the nanotube arrays and metal electrodes, using better nanotube separation techniques, and improving device consistency. In the future, the researchers say that the main challenges will lie in the requirement for extreme engineering control rather than the intrinsic limitations of the nanotubes themselves.

"For high-performance logic applications. currently our target is to replace silicon with carbon nanotubes at 5 nm technology node in 2022-23," Cao told *Phys.org*. "Significant improvements have been achieved, especially in the material aspect, during the past five years. Now we can separate semiconducting and metallic nanotubes with a purity above 99%, and assemble nanotubes at high density. Further improvement to achieve 99.99% purity and reduce defects present during assembly is more or less an engineering control challenge.

"At the same time, more work has to be done to further improve the device, especially at this extremely scaled dimension. For example, device contact resistance has to be reduced with the restriction of limited contact length. A self-aligned process to fabricate sub-10-nm nanotube transistors needs to be established to minimize parasitic capacitance. For thin-film electronics, in my opinion, carbon nanotubes are almost ready to compete with other technologies on the market. Some further improvements are still necessary in term of device reliability and uniformity, but the major challenge is to find the suitable niche application."

More information: Qing Cao, et al. "Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics." *Nature Nanotechnology*. DOI: 10.1038/NNANO.2012.257