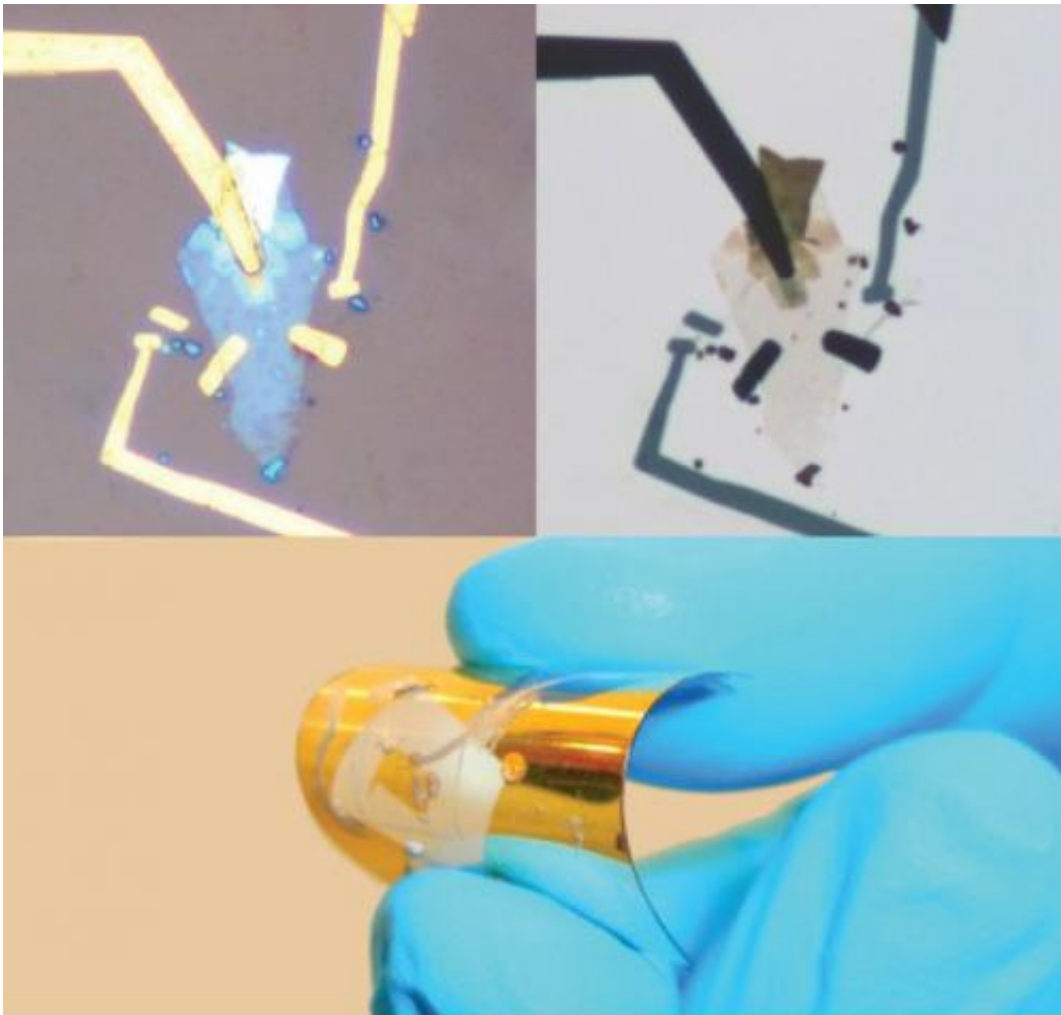


Graphene-based transistor seen as candidate for post-CMOS technology

January 22 2013, by Lisa Zyga



The graphene-based transistor has a very high on/off ratio due to combining two types of transport (tunneling and thermionic), and can operate on a transparent and flexible substrate. Image credit: Thanasis Georgiou, et al. ©2013 Macmillan Publishers Limited. All rights reserved.

(Phys.org)—A new graphene-based transistor in which electrons travel both over a barrier and under it (by tunneling) has exhibited one of the highest performances of graphene-based transistors to date. The combination of the two types of transport enables the transistor to achieve a large difference between its on and off states, giving it a high on/off ratio, which has so far been difficult to achieve in graphene-based transistors. With this advantage, in addition to its ability to operate on transparent and flexible substrates, the new transistor could play a role in post-CMOS devices that are expected to be able to compute at much faster speeds than today's devices.

The researchers from the University of Manchester in the UK, who designed the new graphene-based transistor, have published their study on the device in a recent issue of *Nature* [Nanotechnology](#).

As the researchers explain in their study, other graphene-based transistors have previously been demonstrated, many of which have a sandwich structure with atom-thick sheets of graphene forming the outer layers and a different ultrathin material forming the middle layer. This middle layer can consist of many possible materials. In the current study, the researchers used two-dimensional [tungsten](#) disulphide (WS_2) as the middle layer, which served as an atomically thin barrier between the two layers of graphene.

The biggest advantage of using WS_2 compared to most other barrier materials is that WS_2 's chemical properties allow electrons to cross either by going over the barrier, as in thermionic transport, or under it, as in tunneling. In the off state, very few electrons can cross the barrier by either transport method, but they can cross by one or both methods in the on state.

Switching between the two states involves changing the transistor's gate voltage. A negative gate voltage creates the off state, since it increases

the tunneling barrier height so that few [electrons](#) can cross the barrier. A positive gate voltage switches the transistor to the on state by reducing the tunneling barrier height and—if the temperature is high enough—allowing over-barrier thermionic current as well.

To make the on/off ratio as high as possible, the researchers took advantage of the way the tunneling current's dependence on the voltage changes for different voltage levels. At low voltages and low temperatures, the [tunneling](#) current varies linearly with voltage, but then grows exponentially with the voltage at higher voltages. At this point, thermionic current becomes the dominant transport mechanism.

Using this information to their advantage, the researchers could tune the transistor to achieve an on/off ratio exceeding 1×10^6 at room temperature, which is competitive with the best graphene-based [transistors](#) with any barrier material. Furthermore, this level of performance satisfies the requirements to be a candidate for next-generation post-CMOS electronic devices. Because the new transistor is only a few atomic layers thick, it should be able to tolerate bending and could have potential applications in future flexible, transparent electronic devices.

More information: Thanasis Georgiou, et al. "Vertical field-effect transistor based on graphene–WS₂ heterostructures for flexible and transparent electronics." *Nature Nanotechnology*. [DOI: 10.1038/NNANO.2012.224](#)

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