

New STT-MRAM memory element cuts power consumption of mobile processor by two-thirds

December 13 2012



Figure 1 Cross-section of memory element of Toshiba's perpendicular magnetization type STT-MRAM.

Toshiba Corporation today announced that the company has developed a prototype memory element for a spin transfer torque magnetoresistive random access memory (STT-MRAM) that achieves the world's lowest power consumption yet reported, indicating that it has the potential to surpass the power consumption efficiency of SRAM as cache memory.

Like all digital products, mobile devices, including smartphones and tablet PCs, rely on high-speed memory to supply the main processor with essential instructions and frequently requested data. Until now SRAM has provided the cache-<u>memory solution</u>. However, improving the performance of SRAM to match advances in mobile products results



in increasing current leakage, both during operation and in standby mode, degrading power performance.



Figure 2. Relationship between MRAM processing speed and power consumption.

MRAM, a next-generation memory based on magnetic materials, has emerged as an alternative to SRAM because it is non-volatile, cutting leak current during standby status. However, until now MRAM power consumption has exceeded that of SRAM, throwing up a major barrier to practical application.

Toshiba's new memory element advances the company's pioneering work in STT-MRAM and overcomes the longstanding operating tradeoff by securing improved speed while reducing power consumption by 90 percent. The improved structure is based on perpendicular magnetization and takes element miniaturization to below 30nm.



Introduction of this newly designed "normally-off" <u>memory circuit</u> with no passes for current to leak into cuts leak current to zero in both operation and standby without any specific power supply management.

Toshiba has confirmed the performance of the new STT-MRAM memory element with a highly accurate processor simulator. This modeled application of an STT-MRAM integrating the memory as <u>cache</u> <u>memory</u> and recorded a two-thirds reduction in power consumption by a standard mobile chip set carrying out standard operating functions, a result confirming that the new MRAM element has the lowest <u>power</u> <u>consumption</u> yet achieved. This clearly points the way toward the first MRAM with the potential to surpass SRAM in practical operation.

Going forward Toshiba expects to bring the new memory element to STT-MRAM cache memory for mobile processors integrated into smartphones and tablet PCs, and will promote accelerated research and development toward that end.

This work includes results from the "Normally-off Computing" project funded by Japan's NEDO (New Energy and Industrial Technology Development Organization). Toshiba will present three papers on the new STT-MRAM and its technologies on December 11 and 12 at IEDM, the International Electron Device Meeting held by IEEE in San Francisco from December 10.

Provided by Toshiba

Citation: New STT-MRAM memory element cuts power consumption of mobile processor by two-thirds (2012, December 13) retrieved 28 April 2024 from <u>https://phys.org/news/2012-12-stt-mram-memory-element-power-consumption.html</u>

This document is subject to copyright. Apart from any fair dealing for the purpose of private



study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.