Self-assembled monolayers create p-n junctions in graphene films

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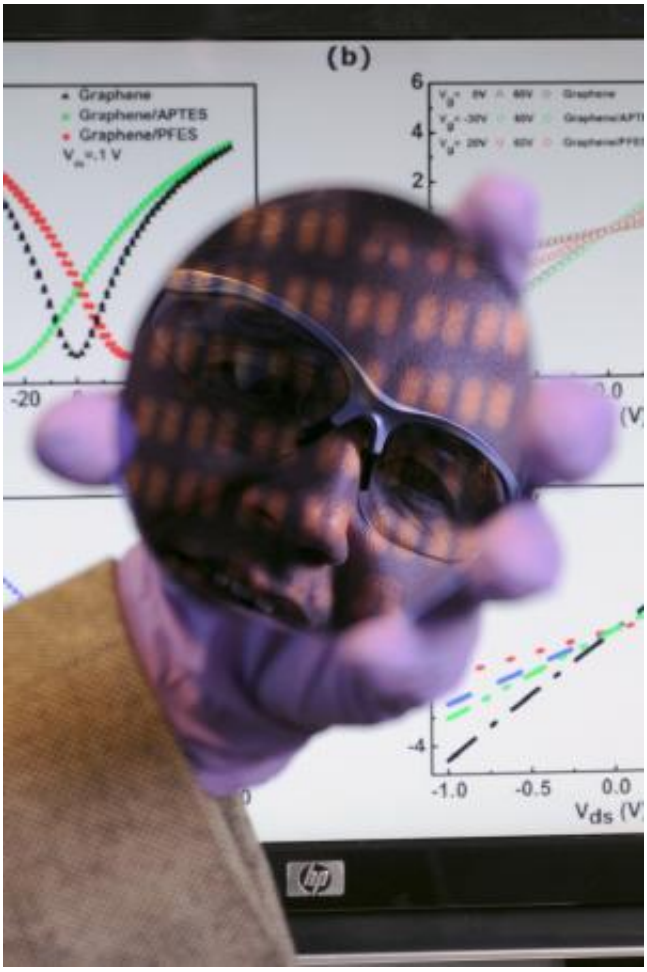


Georgia Tech Professor Clifford Henderson's face is reflected in a wafer containing graphene p-n junctions. The screen in the background shows electrical data measurements. Credit: Georgia Tech Photo: Gary Meek

Researchers are creating graphene p-n junctions by transferring films of the electronic material to substrates that have been patterned by compounds that are either strong electron donors or electron acceptors.

The electronic properties of graphene films are directly affected by the characteristics of the substrates on which they are grown or to which they are transferred. Researchers are taking advantage of this to create graphene p-n junctions by transferring films of the promising electronic material to substrates that have been patterned by compounds that are either strong electron donors or electron acceptors.

A low temperature, controllable and stable method has been developed to dope graphene films using self-assembled monolayers (SAM) that modify the interface of graphene and its support substrate. Using this concept, a team of researchers at the Georgia Institute of Technology has created graphene p-n junctions – which are essential to fabricating devices – without damaging the material's lattice structure or significantly reducing electron/hole mobility.

The graphene was grown on a copper film using chemical vapor deposition (CVD), a process that allows synthesis of large-scale films and their transfer to desired substrates for device applications. The graphene films were transferred to silicon dioxide substrates that were functionalized with the self-assembled monolayers.

Information about creating graphene p-n junctions using self-assembled monolayers was presented on November 28, 2012 at the Fall Meeting of the Materials Research Society. Papers describing aspects of the work were also published in September 2012 in the journals ACS Applied Materials *& Interfaces* and the *Journal of Physical Chemistry C*. Funding for the research came from the National Science Foundation, through the Georgia Tech Materials Research Science and Engineering Center (MRSEC) and through separate research grants.

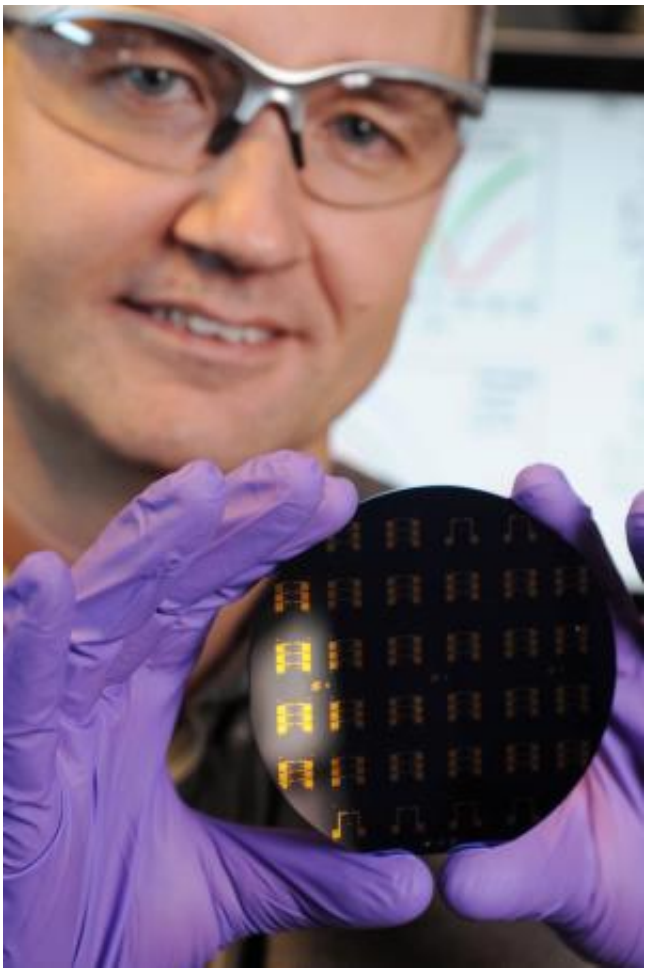
"We have been successful at showing that you can make fairly well doped p-type and n-type graphene controllably by patterning the underlying monolayer instead of modifying the graphene directly," said Clifford Henderson, a professor in the Georgia Tech School of Chemical & Biomolecular Engineering. "Putting graphene on top of self-assembled monolayers uses the effect of electron donation or electron withdrawal from underneath the graphene to modify the material's electronic properties."

The Georgia Tech research team working on the project includes faculty members, postdoctoral fellows and graduate students from three different schools. In addition to Henderson, professors who are part of the team include Laren Tolbert from the School of Chemistry and Biochemistry and Samuel Graham from the Woodruff School of Mechanical Engineering. The project team also includes Hossein Sojoudi, a postdoctoral fellow, and Jose Baltazar, a graduate research assistant.

Creating n-type and p-type doping in graphene – which has no natural bandgap – has led to development of several approaches. Scientists have substituted nitrogen atoms for some of the carbon atoms in the graphene lattice, compounds have been applied to the surface of the graphene, and the edges of graphene nanoribbons have been modified. However, most of these techniques have disadvantages, including disruption of the lattice – which reduces electron mobility – and long-term stability issues.

"Any time you put graphene into contact with a substrate of any kind, the material has an inherent tendency to change its electrical properties," Henderson said. "We wondered if we could do that in a controlled way and use it to our advantage to make the material predominately n-type or p-type. This could create a doping effect without introducing defects that would disrupt the material's attractive electron mobility."

Using conventional lithography techniques, the researchers created patterns from different silane materials on a dielectric substrate, usually silicon oxide. The materials were chosen because they are either strong electron donors or electron acceptors. When a thin film of graphene is placed over the patterns, the underlying materials create charged sections in the graphene that correspond to the patterning.



Georgia Tech Professor Clifford Henderson holds a wafer containing graphene p-n junctions. Credit: Georgia Tech Photo: Gary Meek

"We were able to dope the graphene into both n-type and p-type

materials through an electron donation or withdrawal effect from the monolayer," Henderson explained. "That doesn't lead to the substitutional defects that are seen with many of the other doping processes. The graphene structure itself is still pristine as it comes to us in the transfer process."

The monolayers are bonded to the dielectric substrate and are thermally stable up to 200 degrees Celsius with the graphene film over them, Sojoudi noted. The Georgia Tech team has used 3-Aminopropyltriethoxysilane (APTES) and perfluorooctyltriethoxysilane (PFES) for patterning. In principle, however, there are many other commercially-available materials that could also create the patterns.

"You can build as many n-type and p-type regions as you want," Sojoudi said. "You can even step the doping controllably up and down. This technique gives you control over the doping level and what the dominant carrier is in each region."

The researchers used their technique to fabricate graphene p-n junctions, which was verified by the creation of field-effect transistors (FET). Characteristic I-V curves indicated the presence of two separate Dirac points, which indicated an energy separation of neutrality points between the p and n regions in the graphene, Sojoudi said.

The group uses chemical vapor deposition to create thin films of graphene on copper foil. A thick film of PMMA was spin-coated atop the graphene, and the underlying copper was then removed. The polymer serves as a carrier for the graphene until it can be placed onto the monolayer-coated substrate, after which it is removed.

Beyond developing the doping techniques, the team is also exploring new precursor materials that could allow CVD production of graphene at

temperatures low enough to permit fabrication directly on other devices. That could eliminate the need for transferring the graphene from one substrate to another.

A low-cost, low-temperature means of producing graphene could also allow the films to find broader applications in displays, solar cells and organic light-emitting diodes, where large sheets of graphene would be needed.

"The real goal is to find ways to make graphene at lower temperatures and in ways that allow us to integrate it with other devices, either silicon CMOS or other materials that couldn't tolerate the high temperatures required for the initial growth," Henderson said. "We are looking at ways to make graphene into a useful electronic or opto-electronic material at low temperatures and in patterned forms."

More information: Sojoudi, Hossein, Creating Graphene p-n Junctions Using Self-Assembled Monolayers, Applied Materials & Interfaces, dx.doi.org/10.1021/am301138v and Baltazar, Jose, Facile Formation of Graphene P-N Junctions Using Self-Assembled Monolayers, *The Journal of Physical Chemistry*, dx.doi.org/10.1021/jp3045737

Provided by Georgia Institute of Technology

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