

Samsung delivers strong 14nm FinFET logic process and design infrastructure for advanced mobile SoC customers

December 21 2012

Samsung Electronics today announced that it reached another milestone in the development of 14-nanometer (nm) FinFET process technology with the successful tape-out of multiple development vehicles in collaboration with its key design and IP partners. In addition, Samsung has signed an agreement with ARM for 14nm physical IP and libraries. This agreement is the latest in a series from Samsung and ARM that has delivered production proven SoC enablement. Samsung, together with its ecosystem partners, is in a position to offer leading edge customers a robust design infrastructure to drive an ever expanding advanced mobile SoC market.

"As we move closer to true mobile computing, chip designers are eager to take advantage of the gains in performance and significantly lower power of 14nm FinFET to deliver PC like user experience on a mobile device," said Dr. Kyu-Myung Choi, senior vice president of [System LSI](#) infrastructure design center, Device Solutions Division, [Samsung Electronics](#). "The design complexities at 14nm require complete harmony between the process technology, design methodology, tools and IPs. We are synchronizing all the key elements so our customers can deliver their newest chips to market quickly and efficiently."

As part of its 14nm FinFET development process, Samsung, and its ecosystem partners – ARM, Cadence, Mentor and Synopsys – taped out multiple test chips ranging from a full ARM Cortex-A7 processor

implementation to a SRAM-based chip capable of operation near threshold voltage levels as well as an array of analog IP.

The full ARM Cortex-A7 processor test chip tape-out represents a significant milestone for silicon manufacturing for the fabless ecosystem. The Cortex-A7 implementation on FinFET demonstrates the low-power component of the ARM big.LITTLE™ processor configuration/technology strategy for mobile computing platforms. The Samsung 14nm FinFET enablement for SoC design provides improved leakage and dynamic power advantages to the expanding mobile computing market. This collaboration builds on the long-standing partnership between Samsung and ARM including SoC design enablement for the production proven 32/28nm High-K Metal Gate (HKMG) technology. Enabling SoC design on FinFET allows the continued fast pace of innovation that is the hallmark of the mobile market segment.

The Cortex-A7 processor [test chip](#) was implemented by Cadence in collaboration with ARM and Samsung. Cadence delivered a full RTL-to-signoff flow, building upon a tool set that has been thoroughly tested on 20nm designs requiring automated double patterning. The tight collaboration with Samsung and ARM enabled Cadence to hone its technology for 14nm FinFET designs, paving the way for 14nm market readiness. ARM used Cadence tools to develop the 14nm FinFET libraries, and Cadence tools were also used for a full-flow RTL-to-signoff tapeout of the processor core on Samsung's 14nm FinFET process, as well as chip-level integration and verification.

Samsung used Synopsys tools optimized for FinFET devices to implement additional IP on this vehicle, including low power SRAMs intended to operate with the power supply close to [threshold voltage](#) levels. The move from two-dimensional transistors to three-dimensional transistors introduces several new IP and EDA tool challenges including

modeling. The multi-year collaboration between Samsung and Synopsys has delivered foundational modeling technologies for 3D parasitic extraction, circuit simulation and physical design-rule support of FinFET devices.

Samsung is also extending their work with Mentor to enable a complete solution at 14nm FinFET that addresses customer challenges in design, validation, manufacturing co-optimization, and post-design production ramps. The collaborative efforts leverage the unique capabilities of Samsung's processes, while helping designers deal with the complexities of multi-patterning lithography, FinFET transistors, and more complex reliability requirements.

With its process design kit available to customers today, customers can start designing with models, design rule manuals and technology files that have been developed based on silicon results from previous 14nm FinFET test chips run in Samsung's R&D facilities. This PDK includes design flows, routers and other design enablement features to support new device structures, local interconnects, and advanced routing rules. The investments that Samsung is making into the entire ecosystem at 14nm will give customers early access to all elements of the design infrastructure to accelerate their chip development.

Provided by Samsung

Citation: Samsung delivers strong 14nm FinFET logic process and design infrastructure for advanced mobile SoC customers (2012, December 21) retrieved 3 May 2024 from <https://phys.org/news/2012-12-samsung-strong-14nm-finfet-logic.html>

<p>This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.</p>
--