Semiconductor devices: Under mounting stress

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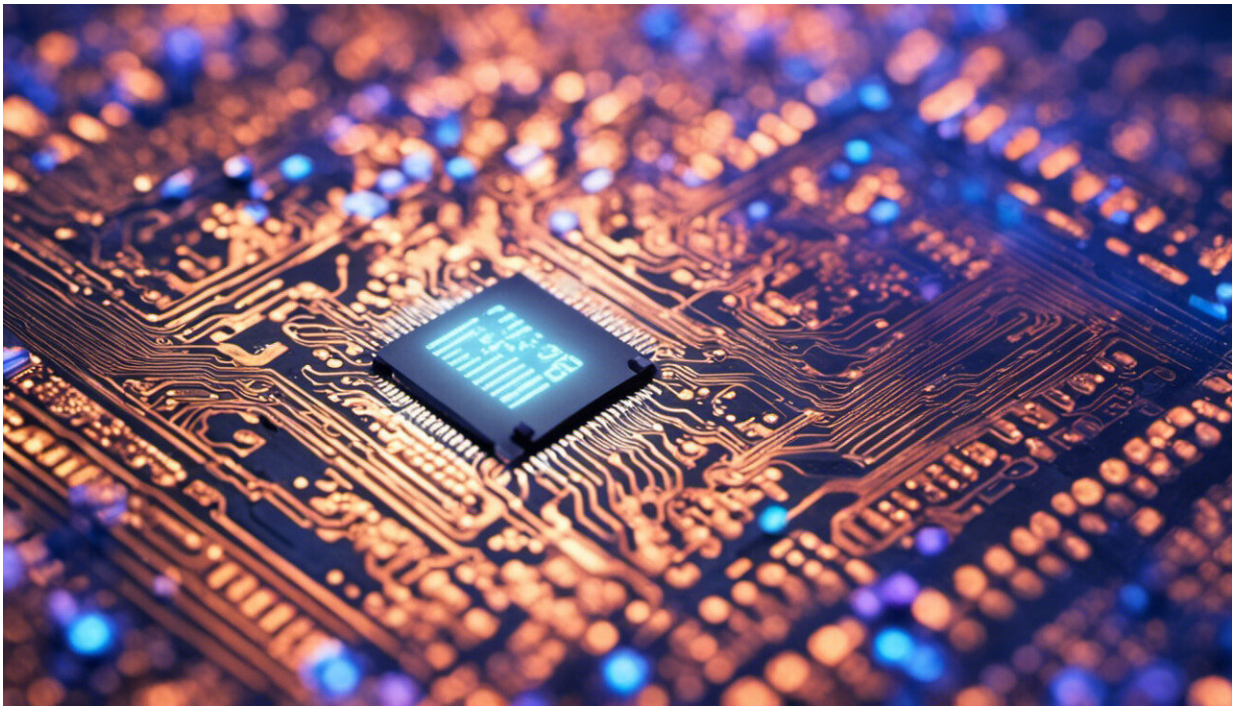

Credit: AI-generated image (disclaimer)

The recently developed ability to measure physical changes in silicon when processed into microelectronic devices could improve fabrication techniques for even smaller circuits.

Thinner semiconductor wafers to house electronic circuits are needed so

that more computing power can be packed into ever-smaller electrical products. Thinning, however, makes the wafers brittle and prone to warping or breaking. A technique for measuring the stress in those chips during production is now available, thanks to developmental work led by Xiaowu Zhang at the A*STAR Institute of Microelectronics, Singapore. The resulting information could enable miniature but robust semiconductor devices.

The conversion from bare wafer to useful device can be an arduous one for a sheet of silicon, particularly when it is only a few millimeters thick. Fabrication processes can involve bombarding the wafer with a beam of ions, dipping it in corrosive acids to etch tiny structures, exposing it to plasmas for cleaning, or coating it in layers of hot metal to create electrical contacts. Then, the wafer must be fixed into a package.

Zhang and his co-workers designed and built stress sensors directly onto a silicon wafer to monitor the strain that such packaging exerts. They took advantage of the piezoresistive effect in silicon—when a force is applied to a silicon wafer, it pushes atoms closer together. In turn, the change in atom distribution alters the way an electrical current passes through the material, which can be measured as a change in resistance. Each stress sensor consisted of 16 resistors (see image). Since the piezoresistive properties of silicon are well known, Zhang and his co-workers could simply convert the changes in resistance to a corresponding change in stress.

By equally distributing 17 such sensors on the sample surface, the researchers monitored the stress in a silicon wafer during a number of common packaging processes. These included coating the wafer in a thin film and attaching a small bump of solder. They also embedded the sensors into a plastic test board, which they dropped repeatedly. Zhang and co-workers also developed a data acquisition system that could monitor the stresses during this impact test.

"Semiconductors are a multibillion-dollar industry," explains Zhang. "This stress data should enable the design of novel packaging technologies and reduce the chance of device damage during processing and during daily use and accidents, such as dropping the device."

Evaluating the stresses on a device wafer during other processes, including a technique known as 'through-silicon via', in which electrical connections are passed all the way through the wafer, will be the next step in the team's research, says Zhang.

More information: Zhang, X., Rajoo, R., Selvanayagam, C. S., Kumar, A., Rao, V. S. et al. Application of piezoresistive stress sensor in wafer bumping and drop impact test of embedded ultrathin device. *IEEE Transactions on Components, Packaging and Manufacturing Technology* 2, 935–943 (2012). ieeexplore.ieee.org/xpl/articl … ontentType=Journals+ %26+Magazines&sortType%3Dasc_p_Sequence%26filter%3DAND%28p_IS_Number%3A6205691%29

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