Samsung will open up on big.LITTLE processor at ISSCC

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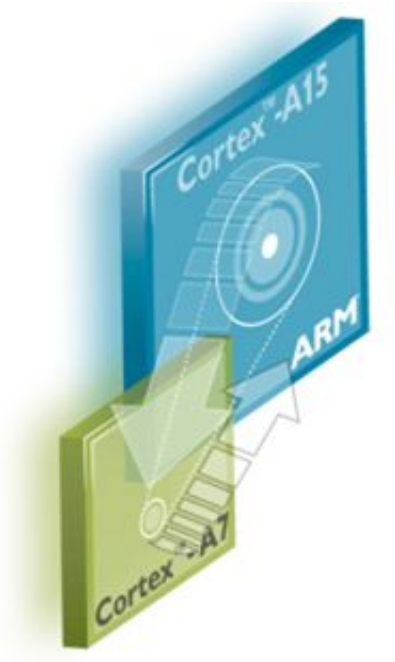

(Phys.org)—Samsung will turn heads at the IEEE International Solid State Circuits Conference (ISSCC) in February when it describes the first mobile applications processor to use ARM's big.LITTLE concept. This is an important opportunity and timing for Samsung, as the ISSCC is a major event for the semiconductor industry. The approach is expected to become widely used in smartphones. Samsung's processor is to use ARM's big.LITTLE architecture. This translates into a SoC built

with a 28 nanometer manufacturing process, with one cluster tuned for sheer performance while the other cluster is optimized for battery life. These are two quad-core clusters, one for high performance applications such as video gaming and the other for energy efficiency.

One cluster runs at 1.8 GHz (Cortex A15) and is geared for high-performance applications; the other runs at 1.2 GHz (Cortex A7) and is tuned for energy efficiency. The pairing of "half powerful" and "half frugal" cores will be suitable for longlasting phones and tablets. An analyst with the Linley Group said that the A7 cores should be capable of handling most smartphone tasks.

According to a white paper from ARM that outlines the big.LITTLE system, the Cortex A15 processor is paired with a "LITTLE" Cortex A7 processor to create a system that can accomplish both high-intensity and low-intensity tasks in the most energy-efficient manner. "By coherently connecting the Cortex-A15 and Cortex-A7 processors via the CCI-400 coherent interconnect, the system is flexible enough to support a variety of big.LITTLE use models, which can be tailored to the processing requirements of the tasks," according to the paper.

The process enables the same application software to switch between them. "By selecting the optimum processor for each task, big.LITTLE can extend battery life by up to 70 percent," claimed ARM. Through these techniques, added ARM, big.LITTLE will provide the opportunity to raise performance and extend battery life in mobile platforms.

What will Intel and NVIDIA reveal about processor plans at the meeting? Intel will not be presenting processor papers at the event, according to a report. Instead, Intel is to describe a scalable 64-lane chip-to-chip interconnect with 1 Tbit/s aggregate bandwidth. NVIDIA is to describe a 20 Gbit/s serial die-to-die link made in 28-nm CMOS.

More information: www.miracd.com/ISSCC2013/PDF/I … 13AdvanceProgram.pdf

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