Researchers develop new packaging technology enabling 90% power combining efficiency

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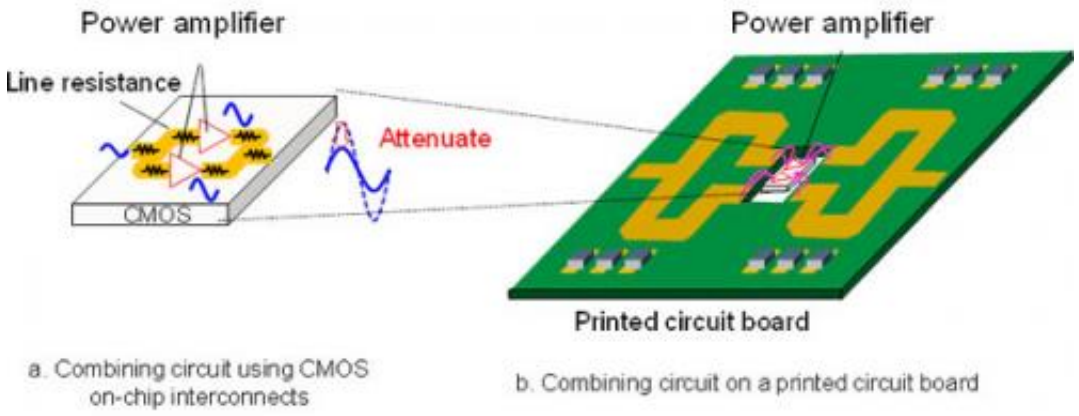


Figure 1: Conventional power amplifier combining circuitry.

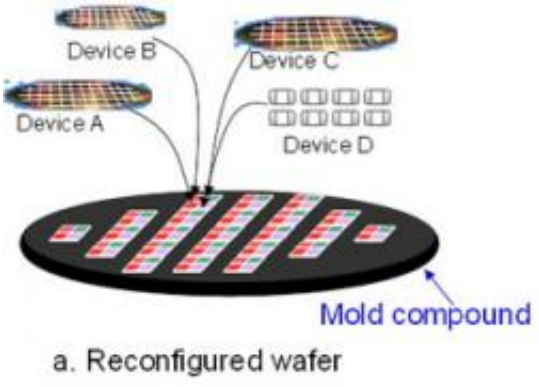
Fujitsu Laboratories today announced the development of a new packaging technology that enables the development of millimeter-wave power amplifiers that can be employed in applications such as automotive radar and wireless communications devices.

One effective way to produce compact, low-cost millimeter-wave transceivers is to integrate high-frequency RF circuitry onto a CMOS(3) chip. At the same time, for normal CMOS circuitry, which operates at low voltages, the high power amplifiers employed in transmitters has proven a challenge that has served as a roadblock to integration. As a

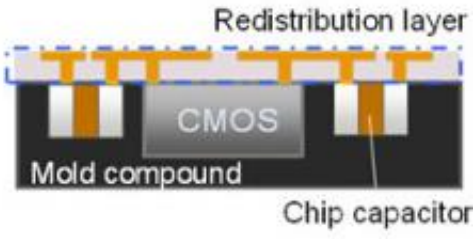
result, there has been a need for a technology that can enable CMOS power amplifiers to achieve higher output.

Fujitsu Laboratories has developed a technology that combines millimeter-wave high-frequency signals generated by multiple power amplifiers within an off-chip module. A prototype module incorporating CMOS power amplifiers based on this technology was able to produce 32 mW output in the 77-GHz frequency band. As a result, it will become possible to develop CMOS millimeter-wave transceivers that employ high-output power amplifiers, which is expected to substantially contribute to the production of smaller, low-cost devices.

In recent years, there has been a widespread adoption of applications employing millimeter-wave technology, such as 77-GHz band automotive radar and 60-GHz band high-capacity wireless communications devices. The RF transceiver ICs presently used in these applications are compound semiconductors(4), which have superior high-frequency characteristics. On the other hand, recent advances in process technologies have brought the operational speed of CMOS technology up to par with that of compound semiconductors, and research is being conducted on ways to implement RF circuitry in CMOS, which can be cheaply manufactured in mass quantities, rather than in compound semiconductors.



a. Reconfigured wafer



b. Cross-sectional view of the integrated package

Figure 2: Integrated package using redistribution layer.

The challenge involved in integrating an RF transceiver into a CMOS chip is in increasing the output of the power amplifier employed in the transmitter. Advances in miniaturization cause a decrease in the power-supply voltages of CMOS circuits, thereby making it difficult to implement high-output power amplifiers. This, in turn, has stood in the way of obtaining power outputs on par with compound semiconductors.

One well-known way to achieve high output from power amplifiers is to array several in parallel and combine their output. If this combining circuitry is fabricated using CMOS on-chip interconnects (see Figure 1a), the thinness of the wiring results in significant line resistance and the power output from the power amplifier is attenuated by roughly 30% by the time it reaches the transmitter, resulting in reduced efficiency. Conversely, if the combining circuit is fabricated on a typical printed-circuit board used in electronic devices (see Figure 1b), the transmission of millimeter-wave signals is impaired due to difficulties in interconnect miniaturization, and the increased size of the module containing the power amplifiers becomes problematic. Therefore, a compact, efficient power combination circuit is desired.

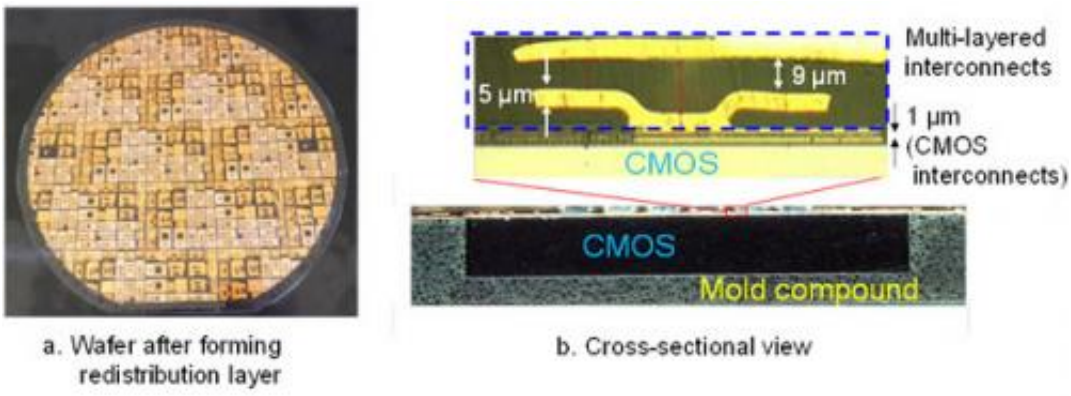


Figure 3: Cross-sectional comparison of CMOS on-chip interconnect with RDL.

Fujitsu Laboratories has developed a new packaging technology (redistribution layer, or RDL, technology) that combines millimeter-wave high-frequency signals generated by power amplifiers within an off-chip module. This, in turn, has enabled the construction of higher output millimeter-wave power amplifiers.

Redistribution layer technology is a packaging technique for semiconductor components in which chip-level semiconductor elements are reconfigured as wafers using a mold compound (Figure 2a) and subsequently formed into a package that connects the electrode patterns between chips through an interconnect process. As the interconnects are formed using a wafer process, fine patterns can be achieved.

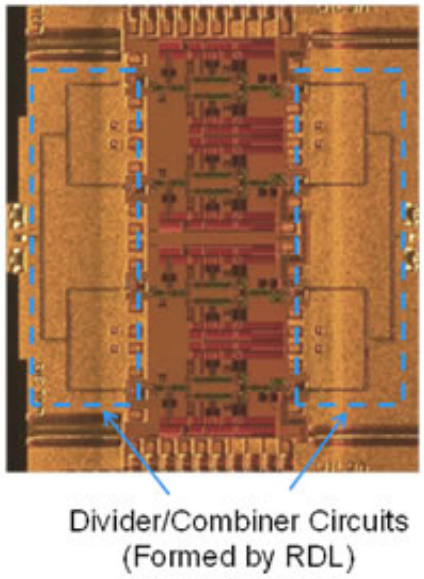


Figure 4: Photo of power amplifier module using RDL technology.

As shown in the cross-sectional view in Figure 2b, a variety of different devices, such as the chip capacitors, can be integrated in the same package, and components can be assembled with high density. Packaging technology using a single-layered RDL has been developed as compact packaging technology for use in applications such as mobile phones, but a packaging structure suited to transmitting millimeter-wave signals has not been developed.

To enable the transmission of high-frequency millimeter-wave signals, Fujitsu Laboratories has developed a power combining circuit that employs multi-layer interconnect technology using multiple interconnection layers (see Figure 3a). As shown in Figure 3b, the interconnection layer formed using an RDL can be more than five times as thick as a typical CMOS on-chip interconnect, thereby reducing line resistance and minimizing losses in the combining circuitry. In addition, by optimizing the thickness of insulation films and the width of interconnect patterns, Fujitsu Laboratories developed a combining

circuit that reduces signal loss to less than 10%.

By adopting this combining circuit in a CMOS power amplifier, it was possible to develop a high-output power amplifier module (see Figure 4). Power output comes from four CMOS power amplifiers arrayed in parallel that each produce 9 mW at 77 GHz, which is channeled to a combining circuit formed using RDL technology. Reducing power loss to 10%—compared to 30% via existing techniques—meant the technology achieved a power combining efficiency of 90%, with power output of 32 mW.

Fujitsu Laboratories has developed a packaging technology that combines CMOS and RDL technology to increase the power output of power amplifiers. By enabling the implementation of power amplifiers on a CMOS chip, which was previously problematic, it will be possible to implement all millimeter-wave RF circuits in CMOS. This is expected to lead to smaller, low-cost RF transceiver chips, as well as low-cost millimeter-wave applications.

Provided by Fujitsu