NRL demonstrates high durability of nanotube transistors to harsh space environment

September 18 2012, by Daniel Parry

A locally etched back-gated field effect transistor (FET) structure with a deposited dielectric layer. Thick dielectric layers are highly susceptible to radiation induced charge build-up, which is known to cause threshold voltage shifts and increased leakage in metal-oxide semiconductor (MOS) devices. To mitigate these effects, the dielectric layer is locally etched in the active region of the back-gated FET. A gate dielectric material is then deposited (depicted in red) over the entire substrate. Credit: U.S. Naval Research Laboratory

U.S. Naval Research Laboratory electronics science and technology engineers demonstrate the ability of single walled carbon nanotube transistors (SWCNTs) to survive the harsh space environment, investigating the effects of ionizing radiation on the crystalline structures and further supporting the development of SWCNT-based nanoelectronics for use in harsh radiation environments.

"One of the primary challenges for space electronics is mitigating the susceptibility of prolonged exposure to radiation that exists in the charged particle belts that encircle Earth," said Cory Cress, materials research engineer. "These are the first controlled demonstrations showing little performance degradation and high tolerance to cumulative ionizing radiation exposure."

Radiation effects take two forms, transient effects and cumulative effects. The former, referred to as single effect transients (SETs), result from a direct strike by an ionizing particle in space that causes a current pulse in the device. If this pulse propagates through the circuit it can cause data corruption that can be extremely detrimental to someone that relies on that signal, such as a person using GPS for navigation. NRL researchers have recently predicted that such effects are nearly eliminated for SWCNT-based nanoelectronics due to their small size, low density, and inherent isolation from neighboring SWCNTs in a device.

The cumulative effects in traditional electronics results from trapped charges in the oxides of the devices, including the gate oxide and those used to isolate adjacent devices, the latter being primary source of radiation-induced performance degradation in state-of-the-art complementary metal–oxide semiconductor (CMOS) devices. The effect is manifested as a shift in the voltage needed to turn the transistor on or off. This initially results in power leakage, but can eventually cause failure of the entire circuit.

By developing a SWCNT structure with a thin gate oxide made from thin silicon oxynitride, NRL researchers recently demonstrated SWCNT transistors that do not suffer from such radiation-induced performance changes. This hardened dielectric material and naturally isolated one-dimensional SWCNT structure makes them extremely radiation tolerant.

The ability for SWCNT-based transistors to be both tolerant to transient and cumulative effects potentially enables future space electronics with less redundancy and error-correction circuitry, while maintaining the same quality of fidelity. This reduction in overhead alone would greatly reduce power and improve performance over existing space-electronic systems even if the SWCNT-based transistors operate at the same speed as current technologies. Even greater benefits are foreseeable in the future, once devices are developed that exceed the performance of silicon-based transistors.

Provided by Naval Research Laboratory