

Intel's plans for quadcore SoC chips discovered

August 29 2012, by Bob Yirka




(Phys.org)—Intel, long dominant on the PC/Windows platform has not been quite so successful in getting its chips inside other machines such as Apple's line of computers, RISC machines, and more recently hand-held devices. Now it appears Intel is ready to mount a serious challenge in all markets with plans for an upgrade to its line of atom processors called,

according to a leaked document, Bay Trail.

The document was apparently [found on Baidu](#) by tech site ComputerBase and details virtually all of Intel's plans for the new chip platform. In the document, purportedly written by people at Intel, it's revealed that the new processor line will include a quadcore System on a Chip (SoC), which, if true, will be a first for Intel, allowing it to play catch-up with rivals in the hand-held market. The document also says the platform will be based on a 22-nanometer architecture, which of course is smaller than anybody else's. SoCs are in a class by themselves because they allow for smaller computers, e.g. hand held devices. In traditional desktop and [laptop computers](#), chips are separated by function with the CPU sitting at the center and directing everything else. Another of those chips, the [Graphics Processing Unit \(GPU\)](#) typically handles, quite obviously, graphics, which in many cases were made by companies not named Intel. With SoCs, everything is integrated into a single chip, which should in theory also make things run faster due to not having to account for communications delays. And the GPU that Intel has embedded in its new chipset appears to bear that out, the document's authors say it's up to seven times faster than anything else out there.

Valleyview 芯片概述



CORE

- 22nm Process Technology Intel® Atom™ processor
- Estimated Speeds - 1.2GHz to 2.4GHz
- 1, 2 and 4 core SKUs
- 512Kb L2 cache per core
- Intel® 64 architecture, Intel® Virtualization Technology, XD Bit
- Extended Temp SKUs
- AEC Q100 Auto Qualified SKUs

MEMORY

- Dual & Single Channel SKUs
- DDR3L-1067/1333, ECC capable in single channel mode
- LPDDR2-800
- Max 8GB
- 32/64 bit width

GRAPHICS, DISPLAY & MEDIA

- 4 Intel Gen 7 Graphics Engines, x2 Display Pipes
- Decode - H.264, MPEG1, MPEG2, MPEG4, VC1/WMV9
- Encode - H.264, MPEG2
- 1 Integrated Imagination Technology® VXD392 Decode Engine
- Decode - H.264, JPEG, VP8

I/O HIGHLIGHTS

- PCI Express® Gen II - Up to x4 lanes
- Intel® High Definition Audio or Low Power Audio
- Image Co-Processor
- HSP-CSI Camera Interface
- Security Engine
 - Secure Boot
 - Blu-Ray® Content Protection (currently for automotive use)

PACKAGES²

- Type-3 27x25mm, 0.593mm Ball Pitch
- Type-4 740F 17x17mm, 0.4mm Ball Pitch
- PRQ Target - Q4'13

I/O Subsystem

| | | | | |
|-------------------------------------------|----------------------|---------------------|---------------------------------|----------------|
| PCIe ¹ Gen 2 Up to x4 | SATA 2.0 Up to x2 | USB 2.0 Up to x4 | USB 3.0 Up to x1 Host/OTG | USB HSIC x1 |
| SPI x2 (1 Allocated for Boot) | I2S x2 | FC x2 | GPIOs | Audio |
| Ethernet iMAC 10/100/1 GigE | UART x2 | SD x1 | SDIO x1 | iMMAC x1 |

System:

- WIFI
- SSD
- ATX
- LAN
- SSD
- SSD
- SSD

SKU Specific - Package & SKU differences will vary feature availability

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Overall the new chipsets, which will continue to be based on Intel's Silvermont (CPU side) architecture will in turn be based on the Bay Trail platform (replacing Cedar Trail) and will come in four varieties: ValleyView T (handheld devices), ValleyView I ([industrial applications](#)), ValleyView M (netbooks) and ValleyView D (desktop computers) and each will be available in a 1, 2 or 4 core configuration running at various clock speeds, providing ultimate versatility. Each will also come with a souped up GPU, which the document says, will bump up video processing four to seven times over existing technology (1080p video at 60 fps).

In addition to scaling down the size of the chipset, Intel has also incorporated out-of-order processing, which means the CPU can process

instructions when they are ready, rather than waiting for slower ones to finish, which of course bumps up overall processing speed.

The document's authors say the new chipsets should be available by the fourth quarter, next year.

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