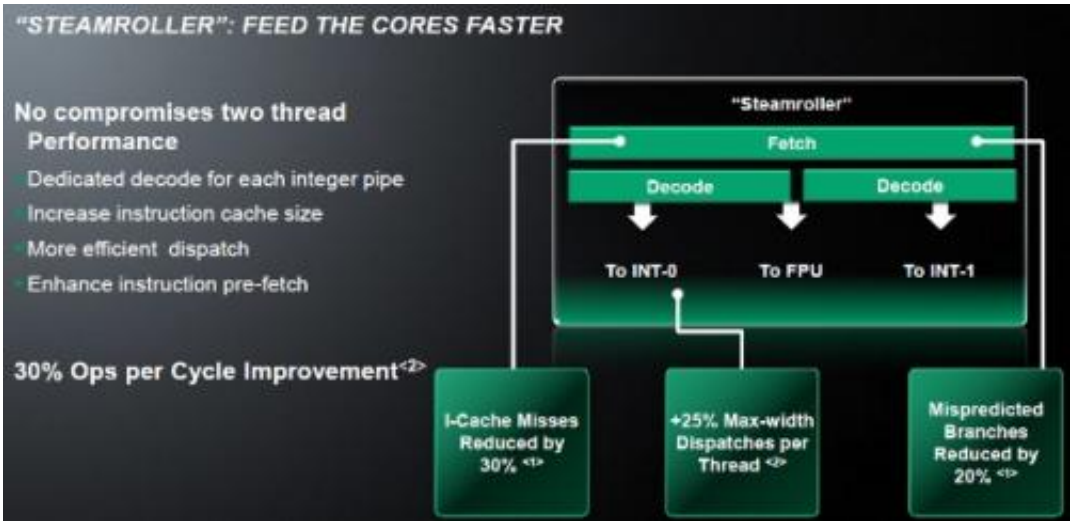
AMD whets Steamroller appetite at Hot Chips

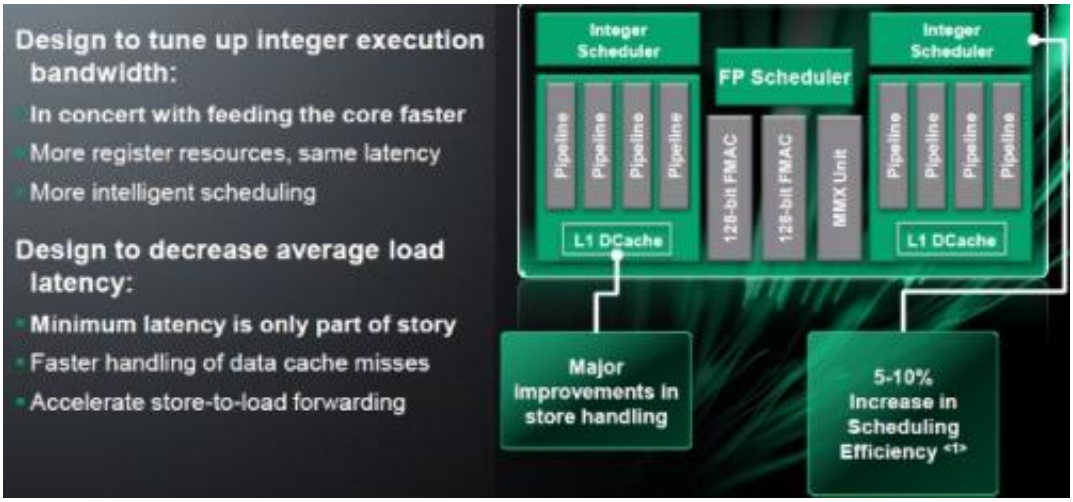
August 29 2012, by Nancy Owano



(Phys.org)—Some might think of AMD as the chip design market underdog, but that underdog raised interest this week when the company's CTO, Mark Papermaster, Senior Vice President & Chief Technology Officer, presented a keynote at the Hot Chips conference, a Cupertino-based symposium focused on high performance chips. Papermaster made some remarks about AMD's upcoming Steamroller x86-64 CPU architecture. Steamroller is a codename for the upcoming CPU architecture from AMD, the third generation of the chip manufacturer's Bulldozer architecture, and will ship next year. Steamroller is in line with the company's general path toward staying

distinctive. AMD has been avoiding speed-racing with competitors such as Intel, to see who can come up with the fastest performing chip. Instead, AMD has focused on being regarded as an outstanding chips designer with a distinctive architecture approach.

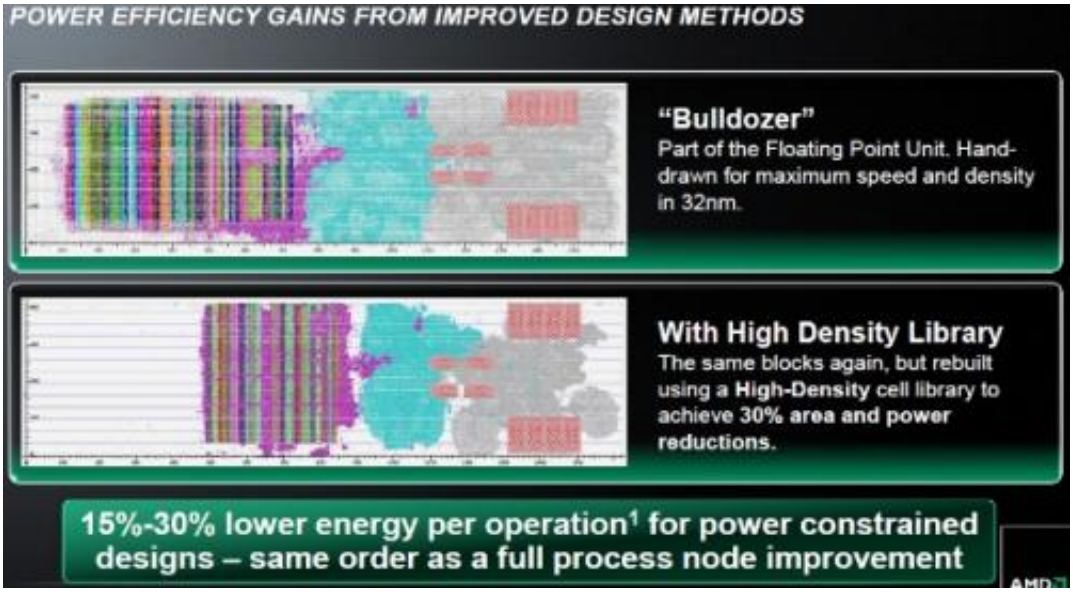
"AMD is leading the quest to develop the types of intuitive devices that understand the users' world," according to Papermaster, "but exist seamlessly in the background environment. It will be built on the perfect marriage of accelerated processing units (APUs), central processing units (CPUs), graphics processing units (GPUs), fixed function logic, a server interconnect fabric and standard software constantly being updated by thousands of developers."



L1 Cache and Integer Scheduler

AMD stays out of the speed race because today's requirements in computing demand something far more. "It's about improving the integer and floating point execution itself, it's about performance per watt," he has said. "It's not a pure speed and feeds race."

Piledriver is AMD x86-64 CPU architecture and Steamroller is to improve on Piledriver's refinements to the original Bulldozer architecture. AMD expects a 15 percent improvement in performance per watt over the Piledriver core.



Steamroller is said to have been worked up as an overall enhancement to efficiencies in processing and power. Tom Verry, in *ExtremeTech,* writes in detail about what Steamroller is to bring:

Steamroller is to carry reduced latency, increased bandwidth, instruction fetching and pipeline optimizations, inter-process communication tweaks, along, and a dynamically-sized L2 cache. *The Register* meanwhile notes that, in the bigger picture, with all three Bulldozer, Piledriver, and Steamroller designs, AMD is sticking with its philosophy of creating "a two-core processor module that has a shared floating point unit and other shared components."