New paths to scaling advanced gatestack and channel material for next-generation CMOS

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In the effort to enhance the advanced metal-high-k gate stack for next-generation logic devices, imec successfully demonstrated higher-k dielectric with Replacement Metal Gate (Metal-Gate-Last) transistors that achieved 200x-1000x reduction in gate leakage relative to leading-edge logic devices in the industry with HfO_2 high-k gate dielectric. To address the process control and scalability of the replacement metal gate for nano-scale devices, imec achieved tight electrical distribution down to 20nm gate length through detailed process optimizations. By providing fundamental insights into work-function influences due to metal intermixing in aggressively-scaled metal gates, imec's research addresses an important source of variability in advanced transistors.

The results were presented at the VLSI Technology Symposium this week in Honolulu, Hawaii, (June 12-15, 2012).

As 3-D transistors like FinFETs are scaled aggressively into 14nm and beyond, many transistor features approach scales of 10s-100s of atoms. The high-aspect ratio and complex topography of FinFETs, make physical analysis and metrology very challenging. Imec's advanced physical analysis laboratory performs very active research on next-generation physical analysis and metrology. Imec was able to apply a novel atom probe tomography technique that enables atomic-level resolution of dopant distribution in nanometer-size FinFET. With clear correlation to transistor electrical performance, the new technique provided unprecedented insights into ultra-shallow junction formation in FinFETs, enabling device design and a clearer understanding of how

dopant atoms are incorporated in nanometer-scale device volumes.

In addition to extensive R&D work on extending the scalability of advanced gate stack and FinFETs, imec also focuses on high-mobility channel transistors. At the VLSI Technology Symposium, imec highlighted record pMOS performance by SiGe quantum well devices. The device is a promising candidate to enable further transistor performance scaling beyond today's strained-Si technology. Recent research work to show the path beyond Si and even beyond Ge was also presented at the VLSI Symposium. In addition, a joint research project with Stanford University investigating the promise of GeSn (Germanium-Tin) channel NMOS devices was highlighted.

Aaron Thean, director of imec's logic device program stated: "We are excited by these excellent results of our advanced transistor program Working closely with our technology partners, this work represents some of the focused imec activities to extend Moore's Law and CMOS technologies. We would also like to thank the VLSI Technology Symposium Committee for their appreciation of our work."

These results were obtained in the framework of imec's core research program on advanced CMOS technologies, in cooperation with imec's key partners programs Globalfoundries, INTEL, Micron, Panasonic, Samsung, TSMC, Elpida, SK hynix, Fujitsu and Sony.

Provided by IMEC

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