

Toshiba announces next-generation superjunction technology for power MOSFETs

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Toshiba America Electronic Components (TAEC) today announced its DTMOS-IV process, a new-generation of superjunction (SJ) technology for power MOSFETs. Products based on the DTMOS-IV technology will make ideal switching devices in switch mode power supplies, lighting ballasts and other power applications that demand a combination of high-speed operation, high-efficiency and low EMI noise.

SJ MOSFETs offer ultra-low on resistance without power loss penalties. As a result, Toshiba's new DTMOS-IV process, which is being deployed in the company's latest family of high-speed, high-efficiency 600V

power MOSFETs, offers on resistance ratings that are up to 30 percent lower than third-generation DTMOS products for the same die size. The benefit is that designers can now choose a 600V MOSFET in a TO-220SIS package with an $R_{DS(ON)}$ of just 0.065Ω , or a similar device in a TO-3P(N) package with an $R_{DS(ON)}$ down to 0.04Ω .

In addition to driving down on [resistance](#), DTMOS-IV has also allowed [Toshiba](#) to minimize [MOSFET](#) output capacitance (C_{oss}) for optimized Switching [Power](#) Supply operation at light load. Furthermore, an optimized gate-drain capacitance (C_{gd}) delivers improved dv/dt switching control, while an optimized $R_{DS(ON)} * Q_g$ figure of merit supports high-efficiency switching. Finally, by supporting lower dv/dt ratings, DTMOS-IV also reduces EMI noise in high-speed switching circuitry.

The DTMOS-IV [technology](#) uses a deep-trench process that results in a narrowing of the lateral SJ pitch, leading to optimized overall performance.

Toshiba's first MOSFETs based on the DTMOS-IV process are available now in an expanded line-up that includes: DPAK, IPAK, D2PAK, I2PAK, TO-220, TO-220SIS, TO-247, TO-3P(N), and TO-3P(L) packages.

Provided by Toshiba

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