

To DDR3: Thanks for the memory but time for DDR4

May 10 2012, by Nancy Owano



(Phys.org) -- Micron Technology is [polishing up its DDR4 memory](#) modules, “sampling” the modules and getting feedback from major customers. The company plans to reach volume production later this year. In brief, Micron is getting ready to bring its DDR4 DRAM modules for market This means the computer industry can expect a new memory standard to make a difference across a range of computing devices, from enterprise computing to so called ultra-thins and tablets. Boise Idaho based Micron this week announced the first piece of its portfolio of DDR4-based modules as the 4-gigabit (Gb) DDR4 x8 part. The announcement said the complete portfolio of DDR4-based modules will include RDIMMs, LRDIMMs, 3DS, SODIMMs and UDIMMs (standard and ECC).

For the “soldered down space,” said Micron, the x8, x16, and x32 components will be available, with initial speeds up to 2400 megatransfers per second (MT/s), increasing to the JEDEC-defined 3200 MT/s. Observers assume that the DDR4 modules will first appear in enterprise machines with ultrathins and tablets up next. Advantages will be twofold; in terms of power savings and performance enhancements. Beyond Boise, one piece of unfinished business is still to be finalized, the JEDEC definition for DDR4. JEDEC stands for Joint Electron Devices Engineering Council and publication of the specification is awaited. JEDEC apparently intends to publish quite soon.

According to JEDEC, “With publication forecasted for mid-2012, JEDEC DDR4 will represent a significant advancement in performance with reduced power usage as compared to previous generation technologies.”

JEDEC said per-pin data rates, over time, will be 1.6 giga transfers per second to 3.2 giga transfers per second. With [DDR3](#) exceeding its expected peak of 1.6 GT/s, it is likely that higher performance levels will be proposed for DDR4 in the future. Also planned in the new standard are a “pseudo open drain interface on the DQ bus, a geardown mode for 2667 Mhz data rates and beyond, bank group architecture, internally generated VrefDQ and improved training modes.” JEDEC will host a DDR4 Technical Workshop following the publication of the standard.

Micron's DDR4 technology was co-developed with Taiwan-based Nanya Technology. Founded in 1995, Nanya does research and development and design, as well as manufacturing, of DRAM products. In 2008, Nanya and Micron entered a joint technology development agreement.

While the JEDEC publication will be complete midyear, [Micron](#) is

wasting no time, with plans to reach volume production of its products in Q4 2012.

Commenting on what to expect with DDR4, Nebojsa Novakovic, writing in *VR-Zone*, said [DDR4](#) has better ways of handling parity and ECC errors than previous memory types, and it can provide recovery from both command and parity errors without crashing the system. Nonetheless, any real deployment will happen in 2014, he said, with AMD and Intel platform support of the new memory.

© 2012 Phys.Org

Citation: To DDR3: Thanks for the memory but time for DDR4 (2012, May 10) retrieved 11 May 2024 from <https://phys.org/news/2012-05-ddr3-memory-ddr4.html>

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.