Researchers prove new circuit pattern-design process, see promise for 14 nanometer design with directed self-assembly

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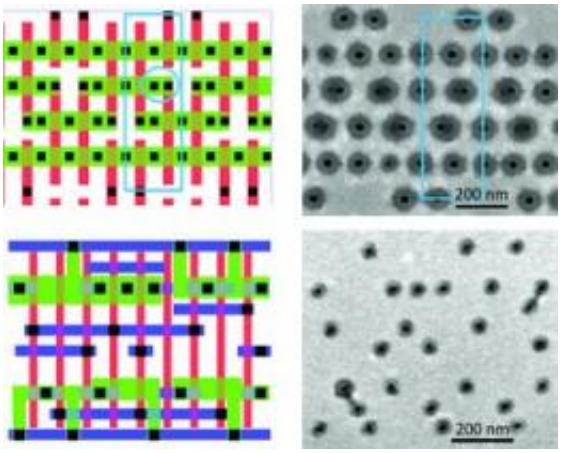

(Phys.org) -- Researchers sponsored by Semiconductor Research Corporation (SRC) announced that they have successfully created contact hole patterns for a wide variety of practical logic and memory devices using a next-generation directed self-assembly (DSA) process. Applying a relatively simple combination of chemical and thermal processes to create their DSA method for making circuits at 22 nanometers (nm), the research team at Stanford University projects that the nanofabrication technique will enable pattern etching for next-generation chips down to 14nm.

In contrast to the current state-of-art lithography methods that rely on increasingly less-accurate steps to shrink transistor and circuit sizes, the achievement at Stanford provides both a more affordable and more environmentally friendly path to fabricating smaller semiconductor devices. The advancement can be utilized for enhancements not only to the electronics industry, but possibly for other nanoscale devices as well.

“This is the first time that the critical contact holes have been placed with DSA for standard cell libraries of VLSI chips. The result is a composed pattern of real circuits, not just test structures,” said H.-S. Philip Wong, lead researcher at Stanford for the SRC-guided research. “This irregular solution for DSA also allows you to heal imperfections in the pattern and maintain higher resolution and finer features on the wafer than by any other viable alternative.”

To build reliable circuits using the new DSA process, the researchers covered a wafer surface with a block copolymer film. Common lithographic techniques were used to carve impressions into the wafer surface, producing a pattern of irregularly placed indentations that serve as templates to guide movement of molecules of the block copolymer into self-assembled configurations.

By varying the shape and size of the guiding templates, manufacturers can space holes more closely than current lithographic methods permit. The resulting closely packed patterns enable the semiconductor industry to build smaller, faster and more energy efficient chips than provided by today’s larger devices.

Environmental improvements over previous generations of manufacturing also are achieved. In order to provide the safest solvents for use in the coating and etching process, the researchers selected polyethylene glycol monomethyl ether acetate (PGMEA) as a healthier and more effective alternative compared to other options.

“This research is a significant contribution to the ability to move ahead on the technological and environmental issues that are important to the industry and the customers it serves,” said Dr. Steve Hillenius, executive vice president for SRC. “In addition, the ability to avoid the cost of lithography tools at $150 million per tool – and it requires a set of multiple such lithographic tools to make the most advanced chips – provides an even more compelling option for patterning.”

A broad range of companies can benefit from the results of the research, including fabless design houses, photoresist companies, tool suppliers and chip manufacturers.

Important next steps remain for the research. Among those is engagement with electronic design automation experts for the purpose of developing software and tools that will enable circuit designers to specify where the holes are to be located on the wafer. This resource for chip designers will allow them to plan without the distraction of where to place the guiding templates, providing the industry with another advantage in addition to the delay of investment in next-generation lithography tools.

More information: Flexible Control of Block Copolymer Directed Self-Assembly using Small, Topographical Templates: Potential Lithography Solution for Integrated Circuit Contact Hole Patterning, *Advanced Materials*, Article first published online: 2 MAY 2012. DOI: 10.1002/adma.201200265

Abstract
Block copolymer directed self-assembly (DSA) using small guiding templates for contact hole patterning in integrated circuits is reported. Flexible and precise DSA control of 25 nm contact holes guided by 66 nm templates for industry-standard 22 nm static random access memory cells is experimentally demonstrated. For 22 nm random logic circuits a

DSA-aware design methodology is developed and the contact holes are achieved with a critical dimension of 15 nm and overlay accuracy of 1 nm.

Provided by Semiconductor Research Corporation