Novel coding technique patented

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Over the past decade, tablet computers and smartphones have taken the world by storm, in no small part due to the way in which they can be switched on almost instantly. The race has been on to develop computers that can similarly be up and running in a matter of moments. Such advances are currently hindered due to the fact that computers need to boot up, as silicon memory chips cannot hold information if the power is turned off. In order to retain information even if the power is turned off, the memory needs to be non-volatile, as is the type of memory commonly found in memory sticks. However, existing memory technologies are expensive, difficult to scale up and often cannot keep up with the demands of current desktop computers. A key contender for future non-volatile memories is the so-called spin-torque transfer magnetic random access memory (STT-MRAM).

Breakthrough in coding and design

Although STT-MRAM devices have been the subject of intense research in the past few years, key hurdles remain. Focusing in particular on the technological aspects of STT-MRAM, Dr. Cai Kui and her non-volatile memory (NVM) Coding Team from the A*STAR Data Storage Institute have now patented an algorithm for correcting errors arising when information is stored and read out incorrectly. Their novel approach significantly enhances the error tolerance of STT-MRAM devices. “This is a breakthrough work that will help provide bigger tolerances and ease the engineering challenges in STT-MRAM material and process development,” says Pantelis Alexopoulos, Executive Director of the Data Storage Institute.

Essentially, STT-MRAM devices encode information through the relative magnetic field orientation of two thin films. The magnetic fields of the two films are oriented parallel or antiparallel to each other. The relative orientation of the fields can be switched because one of the films is a hard magnet whose orientation stays fixed, while the other one is a soft magnet that can be easily realigned. This realignment can be achieved, for example, by an electrical current in which the magnetic property of the electrons — their 'spin' — is polarized in the desired orientation by passing through an appropriate oxide layer in the device. The read-out of the stored information is straightforward as the electrical resistance of a current passing through the device depends on the relative orientation of the two layers. If the magnetic layers are aligned in the same direction, the electrical resistance is smaller than it would be the other way round.

The absolute value of this electrical resistance is more difficult to control and depends on many parameters such as device size or film thickness. Despite on-going efforts to minimize such influences, these parameters inevitably vary from device to device, and as a consequence, the electrical resistance is never really precise. This poses a problem during the conversion of this analogue information into the digital signals used in computing — what should be a digital '0' signal might be sensed as a '1'.

This jeopardizes the usability of memory chips containing billion of these devices, explains Cai: "At present, there is a considerable amount of effort devoted to the device design, material improvement, and process development for STT-MRAM. However, at the same time, there is little work done in the area of coding and signal processing to correct STT-MRAM cell errors." Efforts so far have been limited to conventional error correction procedures that could correct only a very limited number of errors in STT-MRAM devices. In these so-called error correction codes (ECCs), redundancy is built into the encoded

information — the data is converted into more bits than needed. As there is a well-defined relationship between the redundant bits and the input data, it is possible to perform an error correction that enables the retrieval of the stored information even in the presence of errors and noise. However, in these earlier schemes the information is considered strictly as digital 0s and 1s only during the decoding, which means that this hard decoding error correction capability is limited.

For this reason, Cai and colleagues developed a new design of the memory sensing and detection architecture that is based on soft decision decoding. The soft decision decoding goes beyond the strict limitation of 0s and 1s of the bits and also considers the probability of each detected bit being a '0' or '1'. The use of such additional information leads to significantly fewer decoding errors than the hard decision decoding that does not take such probabilities into account.

Improving performance across the board

An important component of the new design is the soft-output channel detector, which measures the probabilities of the bits read out being set as '0' and '1', and feeds this information into the soft decision decoding process of the particular STT-MRAM error correction code utilized here — the so-called low-density parity-check (LDPC) codes.

The improved design also includes a new quantization scheme for STT-MRAM. This is the process that converts the analogue signal into the digital signal. To ensure a high-quality conversion, the analogue information is best encoded into a large number of quantization bits, which greatly increases computational efforts. However, the enhanced error correction procedure means that fewer quantization bits can be used. This not only simplifies the management of such devices but also maximizes the number of information bits that can be stored in a STT-MRAM cell.

Remarkably, Cai and her colleagues have successfully shown that the new scheme achieves a 20% increase in the tolerance towards variations in electrical resistance of the devices. Such relaxed demands greatly ease the manufacturing process of the devices and also will be important when it comes to further reducing STT-MRAM device sizes, as Alexopoulos comments: “DSI’s design of LDPC coding with soft decision decoding for STT-MRAM has a better error correction capability, paving the way for the industry to reduce the cell feature size of future STT-MRAM devices.”

The new error correction approach developed by Cai may well keep STT-MRAM in the running when it comes to replacing flash drives in computers, and lengthy computer boot-up times could soon be a thing of the past. One of the next challenges for the non-volatile memory coding team will be to focus on further scaling of STT-MRAM. “We will further investigate how ECCs with soft decoding can help to improve the various performance of STT-MRAM, and eventually contribute to the scaling of STT-MRAM," says Cai. "We will also design different ECCs for STT-MRAM with different applications."

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