

First patent on low density parity check coding with soft decision decoding for spin-torque transfer MRAM

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Researchers at the A*STAR, Data Storage Institute (DSI), have filed a patent on low-density parity-check (LDPC) coding with soft decision decoding, which is an advanced error correction coding scheme for spin-torque transfer magnetic random access memory (STT-MRAM). This cutting edge technology will shed more light to the limited study on coding and signal processing which is still at its infancy.

In the [memory technology](#) space, STT-MRAM is one of the most promising emerging non-volatile memory (NVM) technologies amongst other technologies such as the [phase change](#) RAM and resistive RAM. A typical cell in the STT-MRAM contains a magnetic tunnelling junction (MTJ) which is the storage element and an access control device. The MTJ contains two ferromagnetic layers, namely the reference layer and the free layer, separated by a tunnelling oxide layer. Information is written on the MTJ by changing the magnetisation direction of the free layer by passing a current through the tunnelling oxide layer. The data stored is either “0”s or “1”s.

Imperfections in the fabrication process greatly affect the reliability of data in STT-MRAM. Process variability causes variation in the tunnelling oxide thickness and cross-section area, which affects both the static and dynamic behaviours of MTJ, resulting in cell errors.

Currently, studies on [error correction](#) codes also known as ECC, for STT-

MRAM found in scientific publications are limited. Conventional error correction codes such as Hamming codes or Bose-Chaudhuri-Hoquenghem (BCH) codes only correct a very limited number of cell errors on STT-MRAM, and the decoding is performed through hard decisions where bits are treated as either “0”s or “1”s.

[DSI](#)'s NVM Coding Team led by Dr. Cai Kui, has developed a novel design of the memory sensing and detection architecture with soft decision decoding, which enables the use of the LDPC code for STT-MRAM. The soft decision decoding works on the probability of each detected bit as being a ‘0’ or ‘1’ (i.e. soft reliability), and hence has less decoding errors than the conventional hard decision decoding. The invention includes a soft-output channel detector that can generate soft reliabilities of the memory readback signals, as well as a novel information theory-based design of the quantisation scheme for STT-MRAM. The soft-output channel detector facilitates the soft decision decoding of the LDPC codes for STT-MRAM. The team is also first to develop a novel quantisation scheme that minimises the number of quantisation bits required by the system. This new scheme does not require tedious and time consuming computer simulations, while at the same time, maximises the number of information bits that can be stored in a STT-MRAM cell.

Compared to conventional error correction code with hard decoding, the new techniques proposed by Dr. Cai's team can decrease the memory sensing error rate and achieve a performance improvement of 20% in terms of maximum affordable resistance spread caused by the fabrication imperfection.

“Currently, there is considerable amount of effort in device design, material improvement, and process development for STT-MRAM. However, there is little work done in the area of coding and signal processing to correct STT-MRAM cell errors,” said Dr Cai. “Our

memory sensing and detection architecture, the quantiser and the soft-output detector can be used for other error correction code with soft decision decoding for STT-MRAM as well.”

“This is a breakthrough work that will help provide bigger tolerances and ease the engineering challenges in STT-MRAM material and process development,” said Dr. Pantelis Alexopoulos, Executive Director of DSI. “As STT-MRAM scales to smaller node, resistance spread and switching current distribution worsens. DSI’s design of LDPC coding with soft decision decoding for STT-MRAM has a better error correction capability, paving the way for the industry to reduce the cell feature size of future STT-MRAM devices.”

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