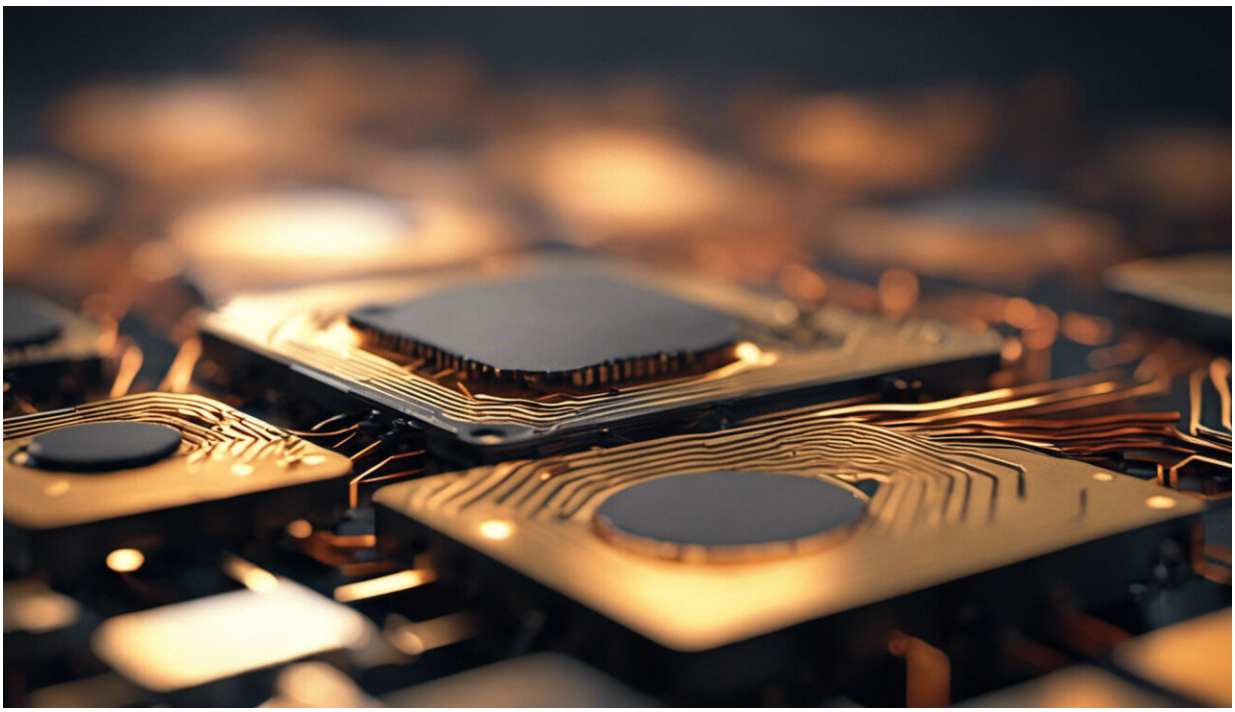
Faster computational methods could simulate the power and signal integrity of next-generation electronic systems

March 29 2012, By Lee Swee Heng



Credit: AI-generated image (disclaimer)

The overall performance of modern computers and communications networks is dependent on the speed of electronic components, such as transistors and optical switches, as well as the quality of the wire network that powers and relays signals between these electronic

components. Power and signal integrity are two important parameters for gauging the quality of a wire network, but simulating these parameters for next-generation electronic systems can take a considerable amount of time, particularly when there is a large number of components involved. Zaw Zaw Oo at the A*STAR Institute for High Performance Computing and co-workers have now significantly decreased the amount of computer time needed by developing a modelling technique that is much more efficient.

In general, there are two different approaches to simulating power and signal integrity of a wire network. One approach is to use exact equations to describe the power and supply networks. This approach is computationally efficient, but the exact equations are difficult to derive for complex networks — for example, those that involve irregularly-shaped ground planes. The other approach is to use numerical methods to describe these complex networks. However, this approach not only requires considerable CPU time and memory, but also becomes unworkable for very large networks.

The researchers therefore used a hybrid approach to combine the benefits of analytical and computational models. They had previously developed a hybrid model capable of describing the power networks in multi-layer circuit boards. In their present work, they extended this model to include the signaling network, as well as loads attached to the circuit board. The researchers considered circuit boards which include one or more pairs of parallel plates that serve as electrical grounds, or deliver power. Their model treats each pair of plates as an individual circuit, in which signal and power flow can be calculated using parallel-plate and transmission line theory. Once each of the individual network have been characterized, they are combined together to describe the entire, original circuit board.

Oo and colleagues tested their model on a case consisting of a multilayer

circuit board measuring 35 mm by 30 mm, which included multiple ground plates, signal traces and vias connecting different layers, and capacitors decoupling different power supply circuits. The reaction of the circuit board to input signals with frequencies up to 20 GHz was calculated using both their new hybrid model, and a numerical finite element model. While the results matched well over the entire frequency range, the new hybrid model required only 48 seconds of CPU time and 0.71 Mb of computer memory to run, compared to 1960 seconds and 74.2 Mb for the finite element approach.

More information: Research article in *IEEE Transactions on Components*, Packaging and Manufacturing Technology

Provided by Agency for Science, Technology and Research (A*STAR)

Citation: Faster computational methods could simulate the power and signal integrity of next-generation electronic systems (2012, March 29) retrieved 7 August 2024 from https://phys.org/news/2012-03-faster-methods-simulate-power-next-generation.html

This document is subject to copyright. Apart from any fair dealing for the purpose of private study or research, no part may be reproduced without the written permission. The content is provided for information purposes only.