Researchers' paper wins Best Paper Award for 2011

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A paper written by Dr. Paul Gratz and his graduate student, Reena Panda, from the Department of Electrical and Computer Engineering at Texas A&M University was selected as one of the best papers from IEEE Computer Architecture Letters in 2011 and will be featured during a special session during The 18th IEEE International Symposium on High-Performance Computer Architecture (HPCA).

All papers that were posted online or appeared in print in *IEEE* Computer Architecture *Letters* in 2011 were eligible for the award, but only a few were chosen by a committee of the journal and HPCA representatives.

Gratz, an assistant professor in the department, and Panda -- along with Dr. Daniel Jiménez from the University of Texas at San Antonio -- won the award for their paper, "B-Fetch: Improving Future Computer System Energy-Efficiency and Performance and through Efficient and Accurate Memory System Speculation."

As in many fields, energy efficiency has become a first order design constraint in modern computer system design. To deal with this problem many computer manufacturers have gone to chip-multiprocessor designs, or CPU chip designs with many processor cores, as a way to lower power consumption. This lower power consumption, however, has come with some cost to performance of individual threads. Programs written in high-level languages, such as C++ and Java, are compiled into a machine-specific assembly language. In assembly, data movement between the

main memory and the processor is explicit and often forms a bottleneck for performance. Chip multiprocessors place an even greater demand on the memory while at the same time avoiding many of the power-hungry speculative techniques used to alleviate memory latency. Data-prefetching, speculatively requesting data before it is needed so that when it is requested by the program it is already available, is a well-known technique to alleviate the effect of memory system latency on performance. However, many data-prefetching schemes either require a high overhead in power and area or do not perform particularly well across all applications.

Their paper proposes a novel data-prefetching scheme known as B-Fetch, which is a mechanism for lightweight, in-order processors that leverage a combination of control path speculation and effectively addresses value speculation. This unique approach yields better performance at approximately one-third the power and area of prior best-of-class data-prefetching schemes.

Gratz is a member of the computer engineering group. He received his Ph.D. in electrical and computer engineering from the University of Texas at Austin in 2008. His research interests include power, reliability and performance in multicore and distributed computer architectures, processor memory systems and on-chip interconnection networks. Honors include receiving a Teaching Excellence Award from The Texas A&M University System.

After the completion of her M.S. Panda accepted a job with Oracle where she currently is working as a processor design engineer.

Provided by Texas A&M University