Fujitsu introduces world's fastest CMOS 14-bit digital-to-analog converter

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FSEU's first 3rd generation high performance Digital to Analog Converter ASSP, the MB86066 'Anakin' DAC, will deliver benefits to, amongst other applications, broadband communications systems, multi-band radio communications systems and test and measurement equipment.

Fujitsu Semiconductor today announced its first 3rd generation high performance Digital to Analog Converter Application Specific Standard Product (ASSP). The MB86066 'Anakin' DAC combines 14-bit resolution with a market-defining conversion rate of up to 12GS/s. The new product will deliver benefits to, amongst other applications, broadband communications systems, multi-band radio communications systems and test and measurement equipment.

Building on Fujitsu's market-leading position for 1 and 1.3GS/s DACs,

which enable superior high Direct-IF architectures, the leap in conversion rate to 12GS/s makes Direct-RF a reality. Such performance is key to enabling true single-platform designs, capable of multi-band as well as multi-mode air interface agnostic signal synthesis. Furthermore, its un-rivaled wide-band performance, comfortably encompassing 50-1,000MHz, meets the needs of all downstream cable modem infrastructure applications. For communications systems infrastructure, this development represents the next step in radio integration, pushing the digital interface closer to the antenna. At the same time it potentially enables simultaneous band and carrier combinations in order to lower system power and cost-per-megabyte transmitted. These capabilities are essential for addressing the insatiable demand for mobile data.

The device integrates two cascaded x2 interpolation filters, reducing the input data required to 3GS/s for full-rate operation. Input data is shared across two parallel LVDS buses, each operating at up to 1.5GS/s, 750MHz DDR. Two further LVDS buses are available to support very-wide band applications, requiring 6GS/s input data. Both interpolation filters can be configured for either low, high or all-pass operation, providing multiple operating and power reduced modes. 15-bit interfaces are implemented to support continuous, per-sample parity checking with automatic error counting.

The device is housed in an 324-ball plastic flip-chip BGA package, measuring 15 x 15mm. Power consumption is only 2.2W when operating at 12GS/s, with both filters enabled, reducing to as low as 950mW at 5.3GS/s for cable modem applications.

For customer specific applications, the DAC core IP, codenamed ‘Jacen’, can be licensed for ASIC solutions, implemented using CS200L, Fujitsu ’s high performance 65nm CMOS technology. This enables the integration of customers’ own digital pre-processing, as well as the adoption of any specific data interface requirements.

To simplify initial device evaluation as well as to enable in-system diagnostics, a Fujitsu proprietary Waveform Memory Module (WMM) is integrated on-chip. The WMM is capable of storing test-vectors of up to 256k samples in length. Full device configuration and control is achieved via a 4-wire serial interface. Development samples are currently undergoing characterisation and qualification testing, with production-ready devices scheduled for Q4 2012.

Source: Fujitsu