# Study explores computing bursts for smartphones

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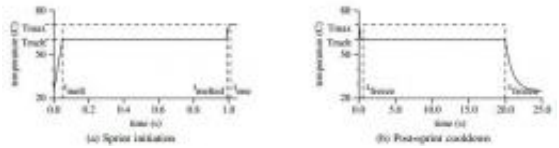

Transient behavior of initiation and termination of sprinting. Image credit: Computational Sprinting, Proceedings of the 18th Symposium on High Performance Computer Architecture (HPCA 2012).

(PhysOrg.com) -- A study team from the computer science and engineering departments at University of Pennsylvania and University of Michigan are tackling smartphone performance with an idea about chips that are designed for what they say is computational sprinting. “Our approach called computational sprinting is aimed at mobile environments like smartphones, where many interactive applications are characterized by short bursts of computational demand punctuated by long idle periods waiting for user input,” they said.

What they have in mind are computer chips with over 12 processing cores rather than multicore chips with two or four. The phone would use a single core to carry out normal operations but it would utilize all cores for heavy-duty computation to ensure the tasks are done with speed.

In their paper, “Computational Sprinting,” the authors point to the

present-day performance constraints in smartphones. In mobile settings, said the researchers, “Many current and emerging interactive applications are characterized by short bursts of intense computation punctuated by long idle periods.”

What led to their research is their recognition that processors today, with their heat sinks and energy delivery systems, are made for sustained performance, which is ideal for batch-mode high-performance computing but not ideal for interactive workloads requiring responsiveness in seconds once the user has initiated a command.

They posed the question, what would a system look like if designed to provide responsiveness during bursts rather than focusing on sustained performance? They report results where, after simulating a sprinting chip, they saw a significant performance boost. As the concept is still in lab stage and a physical version is yet to be built, they acknowledge “parallel computational sprinting” still poses engineering challenges in cost, thermal materials, packaging and power supply.

Nonetheless, they said, “Our study indicates that it is feasible to capture the responsiveness of a 16W chip within the engineering constraints of a 1W mobile device via parallel computational sprinting.”

In reaction to their research, Michael Taylor, computer science professor at the University of California, San Diego, said in Newscientist that the challenge will be for manufacturers to find phase-change materials (PCMs) that are compact enough for a mobile device but still absorb heat without the phone becoming too hot.

The study team, Arun Raghavan, Yixin Luo, Anuj Chandawalla, Marios Papaefthymiou, Kevin P. Pipe, Thomas F. Wenisch and Milo M. K. Martin are to present “Computational Sprinting” in the Proceedings of the 18th Symposium on High Performance Computer Architecture

(HPCA 2012), which takes place from February 25 to 29 in New Orleans.

**More information:** www.cis.upenn.edu/acg/sprinting/