Darpa seeks new power dynamic for continuation of Moore's Law

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Computational capability is an enabler for nearly every military system. But computational capability is increasingly limited by power requirements and the constraints on the ability to dissipate heat. One particular military computational need is found in intelligence, surveillance and reconnaissance systems where sensors collect more information than can be processed in real time. To continue to increase processing speed, new methods for controlling power constraints are required.

In the past, computing systems could rely on increasing computing performance with each processor generation. Following Moore's Law, each generation brought with it double the number of transistors. And

according to Dennard's Scaling, clock speed could increase 40 percent each generation without increasing power density. This allowed increased performance without the penalty of increased power.

"That expected increase in processing performance is at an end," said DARPA Director Regina E. Dugan. "Clock speeds are being limited by power constraints. Power efficiency has become the Achilles Heel of increased computational capability."

DARPA's Power Efficiency Revolution for Embedded Computing Technologies (PERFECT) program seeks to improve power efficiency for embedded computer systems, providing more computing per watt of electrical power. To increase awareness of this program and attract potential researchers, DARPA has scheduled a Proposers' Day workshop Feb. 15 in Arlington, Va. Proposers' Day details are available through the Special Notice located here.

As transistor operating voltages approach logic threshold voltage, device operating characteristics change dramatically, decreasing both reliability and maximum operating frequency. Since reliability and operating frequency are critical to its user base, commercial industry has only limited ability to reduce operating voltage to avoid these clock frequency decreases. PERFECT seeks revolutionary approaches to processing-power efficiency to overcome these limitations. This approach includes near threshold voltage operation and massive heterogeneous processing concurrency, combined with techniques to effectively use the resulting concurrency and tolerate the resulting increased rate of soft errors.

Provided by DARPA