Vertical silicon nanowires for nonvolatile memory devices

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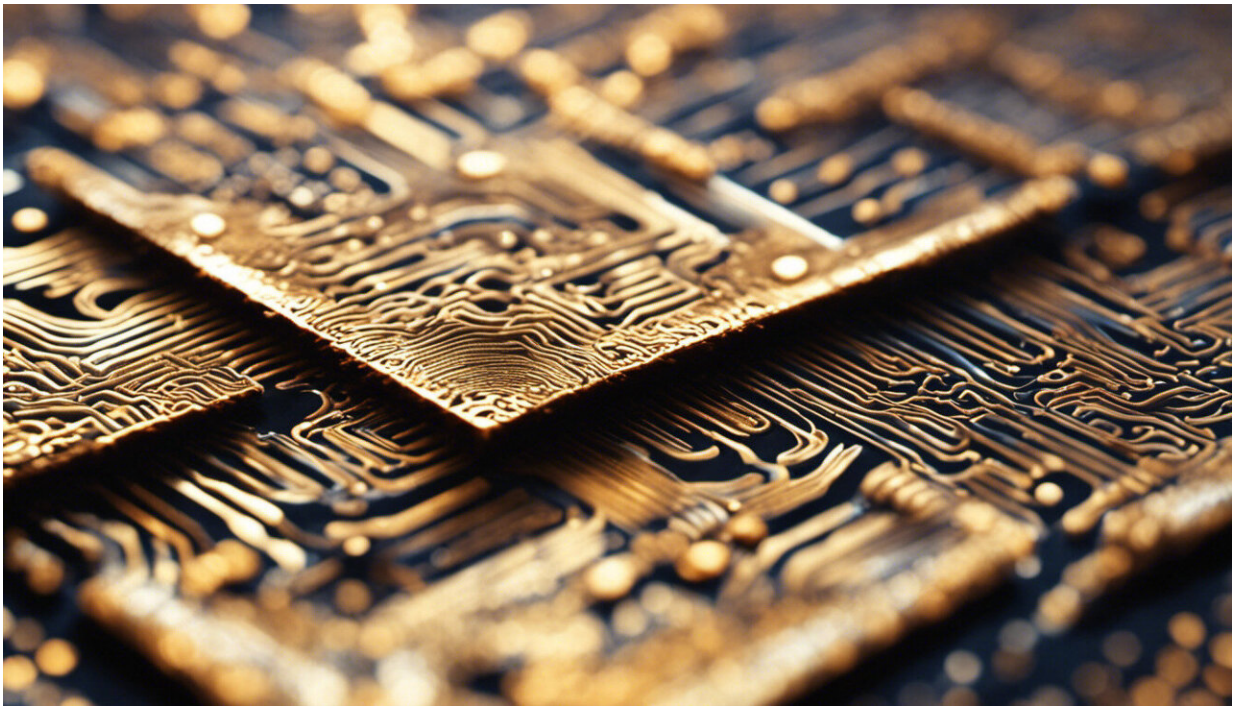

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As electronic devices become smaller and more sophisticated, the search for compact nonvolatile memory becomes increasingly important. However, conventional silicon technologies, such as complementary metal-oxide-semiconductor (CMOS) and floating gate flash memory, are fast reaching their scaling limit. Further miniaturization could seriously

affect their performance and stability.

Navab Singh and co-workers at the A*STAR Institute of Microelectronics and the Nanyang Technical University of Singapore have now created a highly scalable method for storing data using vertical nanowires. Their device contains none of the 'junctions' commonly used in conventional silicon technologies and has a much smaller footprint.

In a CMOS device, a junction is the boundary of a p-type and an n-type semiconductor created by adding functional impurities selectively into the semiconductor crystal. In the new device, Singh and co-workers created an 'electrical' junction by carefully selecting the gate material based on their work function and eliminating the need for any doped junction inside the silicon nanowires. The charges are stored in a nitride thin film sandwiched between the surrounding gate and the wire, separated by thin oxide layers on both sides.

"The nanowires are uniformly doped without junctions and conduction through them is controlled by a gate surrounding their central portion," explains Singh. "The gate material is selected such that when there is zero potential applied on the gate, the wire is fully depleted of carriers and the current cannot flow, creating an OFF state."

The amount of charge tunneled into the nitride from the nanowire also influences the current through the wire. The different current values, namely 'high' or 'low', caused by different numbers of charges trapped and their position in the nitride, signify different data bits.

"Our devices, being vertical, enjoy multi-bit data storage per cell because charges trapped at different locations in the nitride do not interfere with each other, meaning they can remain far apart even with aggressive scaling of the footprint," says Singh. "Such interference has been one of the key challenges in scaling the flash memory.

Furthermore, we can put multiple cells on a single wire like a multi-storey building, allowing even more bits being stored per nanowire."

The devices are sensitive to variations, so the researchers had to run the process under tight controls. In particular, the vertical nanowires must be uniform in shape due to differences between the top and bottom storage bits if tapered.

Despite these challenges, Singh believes the junctionless system may hold the key to future memory storage for data centers, computers and mobile devices. What's more, by removing the doped junctions, devices could be much simpler and cheaper to make.

More information: Research article in Electron Device Letters

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