

IBM researchers demonstrate future of computing with graphene, racetrack and carbon nanotube breakthroughs

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Today at IEEE International Electron Devices Meeting, IBM scientists unveiled several exploratory research breakthroughs that could lead to major advancements in delivering dramatically smaller, faster and more powerful computer chips.

For more than 50 years, computer processors have increased in power and shrunk in size at a tremendous rate. However, today's chip designers are hitting physical limitations with Moore's Law, halting the pace of product innovation from scaling alone.

With virtually all electronic equipment today built on complementary-symmetry metal-oxide-semiconductor (CMOS) technology, there is an urgent need for new materials and circuit architecture designs compatible with this engineering process as the technology industry nears physical scalability limits of the silicon transistor.

Following years of key physics advances previously only achieved in a laboratory, IBM scientists successfully integrated the development and application of new materials and logic architectures on 200mm (eight inch) diameter wafers. These breakthroughs could potentially provide a new technological basis for the convergence of computing, communication, and consumer electronics.

Racetrack Memory

[Racetrack memory](#) combines the benefits of magnetic hard drives and solid-state memory to overcome challenges of growing memory demands and shrinking devices.

Proving this type of memory is feasible, today IBM researchers are detailing the first Racetrack memory device integrated with CMOS technology on 200mm wafers, culminating seven years of physics research.

The researchers demonstrated both read and write functionality on an array of 256 in-plane, magnetized horizontal racetracks. This development lays the foundation for further improving Racetrack memory's density and reliability using perpendicular magnetized racetracks and three-dimensional architectures.

This breakthrough could lead to a new type of data-centric computing that allows massive amounts of stored information to be accessed in less than a billionth of a second.

Graphene

This first-ever CMOS-compatible [graphene](#) device can advance wireless communications, and enable new, high frequency devices, which can operate under adverse temperature and radiation conditions in areas such as security and medical applications.

The graphene integrated circuit, a frequency multiplier, is operational up to 5 GHz and stable up to 200 degrees Celcius. While detailed thermal stability still needs to be evaluated, these results are promising for graphene circuits to be used in high temperature environments.

New architecture flips the current graphene transistor structure on its

head. Instead of trying to deposit gate dielectric on an inert graphene surface, the researchers developed a novel embedded gate structure that enables high device yield on a 200mm wafer.

Carbon Nanotubes

IBM researchers today demonstrated the first transistor with sub-10 nm channel lengths, outperforming the best competing silicon-based devices at these length scales.

While already being considered in varied applications ranging from solar cells to displays, it is expected that computers with in the next decade will use transistors with a channel length below 10 nm, a length scale at which conventional silicon technology will have extreme difficulty performing even with new advanced device architectures. The scaled [carbon nanotube](#) devices below 10nm gate length are a significant breakthrough for future applications in computing technology.

While often associated with improving switching speed (on-state), this breakthrough demonstrates for the first time that carbon nanotubes can provide excellent off-state behavior in extremely scaled devices-- better than what some theoretical estimates of tunneling current suggested.

Provided by IBM

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