

# **New EU project targets first 100GHz optical RAM silicon chips**

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A new EU project that aims to develop a 100 gigabits per second (Gbps) optical random access memory (RAM) chip has just kicked off. This chip will be the first of its kind.

There are six project partners participating in RAMPLAS ('100 Gbps optical RAM on-chip: silicon-based, integrated optical RAM enabling high-speed applications in computing and communications'). The project has been funded in part by almost EUR 2 million under the 'Information and communication technologies' (ICT) Theme of the EU's Seventh Framework Programme (FP7).

The project partners, who hail from Germany, Greece, the Netherlands and Finland, will re-examine the fundamental principles of the RAM computer data storage form. They will also lay the foundations for new optical RAM technology and for optical RAM-enabled ultra-fast computing architectures.

For over two decades, the gap between processor and memory speed has continued to increase; this phenomenon is commonly referred to as the 'Memory Wall'. Current electronic RAM is too slow to keep up with increased processor speeds, and this creates a bottleneck in system performance.

Step in the RAMPLAS consortium with their objective of developing the first 100 Gbps optical RAM chips exploiting photonic integration technologies at the [Silicon-on-Insulator](#) (SOI) platform. SOI technology

involves using a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics; this reduces parasitic device capacitance and improves performance

The RAMPLAS team hope to increase RAM access speeds by two orders of magnitude and decrease the [power consumption](#) by 50% compared to existing state-of-the-art electronic RAM modules. Another aim of the three-year project is to foster a new framework for required disciplines for RAM's effective application in the world of computing, communications, and test and [measurement technologies](#).

RAMPLAS takes a cross-disciplinary approach and blends innovation in computer science, optical design, photonic integration and semiconductor physics. It aims to provide the theoretical foundations of optical RAM and to introduce novel optical RAM circuit designs. A building-block approach will associate circuit design with physical layer parameters; using hetero-integration techniques will increase integration density on established SOI technology. Multi-bit RAM chips with up to 64-bit capacity are envisaged to pave the way to densely integrated optical RAM and kilobyte capacities.

RAMPLAS addresses the entire framework for optical RAM-enabled computing. Fundamental connections between content distributed networks and chip-level multiprocessing (CMP) architectures will be established to introduce the concepts the team develop.

New three-dimensional (3D) cache-mapping algorithms will be researched, exploiting the wavelength dimension in memory addressing for reconfigurable set-associative cache mapping towards maximising cache hit ratio.

The research outcomes of RAMPLAS will be evaluated in a solid proof-

of-concept validation plan based both on simulations and experiments.

The project partners are led by the Centre for Research and Technology Hellas, (CERTH) in Greece. The other members are the Technische Universität (TU) Berlin in Germany, the Technical Research Centre of Finland (VTT), PhoeniX Software in the Netherlands, the Institute of Communication and Computer Systems (ICCS) in Greece and the Tampere University of Technology in Finland.

**More information:** [www.ict-ramplas.eu/](http://www.ict-ramplas.eu/)

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