Controlling silicon evaporation allows scientists to boost graphene quality

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Georgia Tech graduate students Yike Hu and John Hankinson observe a high temperature furnace used to produce graphene on a silicon carbide wafer. Credit: Image Courtesy of Gary Meek

Scientists from the Georgia Institute of Technology have for the first time provided details of their "confinement controlled sublimation" technique for growing high-quality layers of epitaxial graphene on silicon carbide wafers. The technique relies on controlling the vapor pressure of gas-phase silicon in the high-temperature furnace used for fabricating the material.

The basic principle for growing thin layers of graphene on silicon carbide requires heating the material to about 1,500 degrees Celsius under high vacuum. The heat drives off the silicon, leaving behind one or more layers of graphene. But uncontrolled evaporation of silicon can produce poor quality material useless to designers of electronic devices.

"For growing high-quality graphene on silicon carbide, controlling the evaporation of silicon at just the right temperature is essential," said Walt de Heer, a professor who pioneered the technique in the Georgia Tech School of Physics. "By precisely controlling the rate at which silicon comes off the wafer, we can control the rate at which graphene is produced. That allows us to produce very nice layers of epitaxial graphene."

De Heer and his team begin by placing a silicon carbide wafer into an enclosure made of graphite. A small hole in the container controls the escape of silicon atoms as the one-square-centimeter wafer is heated, maintaining the rate of silicon evaporation and condensation near its thermal equilibrium. The growth of epitaxial graphene can be done in a vacuum or in the presence of an inert gas such as argon, and can be used to produce both single layers and multiple layers of the material.

"This technique seems to be completely in line with what people might one day do in fabrication facilities," de Heer said. "We believe this is quite significant in allowing us to rationally and reproducibly grow graphene on silicon carbide. We feel we now understand the process, and believe it could be scaled up for electronics manufacturing."

The technique for growing large-area layers of epitaxial graphene was described this week in the Early Edition of the journal *Proceedings of the National Academy of Sciences*. The research has been supported by the National Science Foundation through the Georgia Tech Materials Research Science and Engineering Center (MRSEC), the Air Force

Office of Scientific Research, and the W.M. Keck Foundation.

The paper also describes a technique for growing narrow graphene ribbons, a process de Heer's group has called "templated growth." That technique, which could be useful for making graphene interconnects, was first described in October 2010 in the journal *Nature Nanotechnology*.

A high temperature furnace is used to produce graphene on a silicon carbide wafer. Credit: Image courtesy of Gary Meek

The templated growth technique involves etching patterns into silicon carbide surfaces using conventional nanolithography processes. The patterns serve as templates directing the growth of graphene structures on portions of the patterned surfaces. The technique forms nanoribbons of specific widths without the use of electron beams or other destructive cutting techniques. Graphene nanoribbons produced with these templates

have smooth edges that avoid problems with electron scattering.

Together, the two techniques provide researchers with the flexibility to produce graphene in forms appropriate to different needs, de Heer noted. Large-area sheets of graphene may be grown on both the carbon-terminated and silicon-terminated sides of a silicon carbide wafer, while the narrow ribbons may be grown on the silicon-terminated side. Because of different processing techniques, only one side of a particular wafer can be used.

The Georgia Tech research team - which includes Claire Berger, Ming Ruan, Mike Sprinkle, Xuebin Li, Yike Hu, Baiqian Zhang, John Hankinson and Edward Conrad – has so far fabricated structures as narrow as 10 nanometers using the templated growth technique. These nanowires exhibit interesting quantum transport properties.

"We can make very good quantum wires using the templated growth technique," de Heer said. "We can make large structures and devices that demonstrate the Quantum Hall Effect, which is important for many applications. We have demonstrated that templated growth can go all the way down to the nanoscale, and that the properties get even better there."

Development of the sublimation technique arose from efforts to protect the growing graphene from oxygen and other contaminants in the furnace. To address the quality concerns, the research team tried enclosing the wafer in a graphite container from which some silicon gas was permitted to leak out.

"We soon realized that graphene grown in the container was much better than what we had been producing," de Heer recalled. "Originally, we thought it was because we were protecting it from contaminants. Later, we realized it was because we were controlling the evaporation of silicon."

Epitaxial graphene may be the basis for a new generation of high-performance devices that will take advantage of the material's unique properties in applications where higher costs can be justified. Silicon, today's electronic material of choice, will continue to be used in applications where high-performance is not required, de Heer said.

Though researchers are still struggling to design nanometer-scale epitaxial graphene devices that take advantage of the material's unique properties, de Heer is confident that will ultimately be done.

"These techniques allow us to make accurate nanostructures and seem to be very promising for making the nanoscale devices that we need," he said. "While there are serious challenges ahead for using graphene in electronics, we have overcome roadblocks before."

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