Imec achieves breakthroughs in enabling future DRAM and RRAM

July 12 2011

In the frame of its research on future memory architectures, imec has made breakthroughs for both DRAM and RRAM memories. For DRAM, MIMcap (metal-insulator-metal capacitor) was established as a clear candidate for 1X DRAM scaling. Imec demonstrated a record low leakage current and was able to explain the mechanism for leakage reduction, showing the path for further potential improvement. For Resistive RAM (RRAM), imec built a model to understand the properties of the filaments that result in a stable RRAM operation. Such fundamental understanding of the filament properties is key to bridge the gap in the development of RRAM as a successor memory technology.

One of the major technical challenges for the DRAM industry is the difficulty to maintain target leakage currents at lower Effective Oxide Thicknesses (EOT) to meet the DRAM capacitor scaling roadmap. Recently, imec demonstrated a novel RuOx/STO/TiN stack that showed a 100x reduction in leakage with DRAM MIMcap compatible dielectrics at 0.4nm equivalent oxide thickness (EOT). Now, imec has achieved a further 10x improvement by optimizing the stack, resulting in a record leakage current density (JG) of 2x10-8A/cm^2 at 0.4nm EOT. In addition, imec was able to explain the mechanism of leakage reduction. This allowed a path to demonstrate a further potential through lowering the trap density, to a theoretical leakage current density (JG) limit for trap-free STO of 10-15A/cm^2 at ~0.4nm EOT. These results demonstrate that the STO-based stack is a promising technology for DRAM scaling.

RRAM is a promising concept for future non-volatile memories. In RRAM, a dielectric, which is normally insulating, can be made conductive through a filament or conduction path formed by applying a sufficiently high voltage. Imec now has made breakthroughs in understanding the properties of the filaments. Imec established a.o. that the minimal achievable current after reset depends on the physical nature of the filaments, resulting in a direct method to predict that current from the filament properties. With these results, it is now possible to choose the desired properties of the filaments to ensure a stable RRAM operation.

These results were obtained in cooperation with imec's key partners in its core CMOS programs Globalfoundries, INTEL, Micron, Panasonic, Samsung, TSMC, Elpida, Hynix, Fujitsu and Sony.

Provided by IMEC

Citation: Imec achieves breakthroughs in enabling future DRAM and RRAM (2011, July 12) retrieved 25 April 2024 from https://phys.org/news/2011-07-imec-breakthroughs-enabling-future-dram.html