Imec demonstrates 3D integrated DRAM-on-logic for low-power mobile applications

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Logic IC stacked on DRAM IC, connected using TSVs and microbumps

Imec and its 3D integration partners have proven the potential of 3D integration of a commercial DRAM chip on top of a logic IC for next-generation low-power mobile applications. Imec's applied 3D EDA (electronic design automation) tools including thermal models have proven to be valuable means to design next-generation 3D stacked ICs.

The 3D stack resembles as close as possible to future commercial chips. It consists of imec's proprietary logic CMOS IC on top of which a commercial DRAM is stacked using through-silicon vias (TSVs) and micro-bumps. Heaters were integrated to test the impact of hotspot on DRAM refresh times. And, the chip contains test structures for monitoring thermo-mechanical stress in a 3D stack, ESD (electro-static discharge) hazards, electrical characteristics of TSVs and micro-bumps,

fault models for TSVs, etc.

Imec's 3D integrated DRAM-on-logic demonstrator showed that a minimum die thickness of 50µm is required to deal with local hot spots on the logic die, which are generated by local power dissipation. Due to the strongly reduced lateral heat spreading capability of thin die, these hot spots are higher in temperature and more confined if the die thickness is reduced.

The hot spots on the logic die cause local temperature increases in the memory die. This may cause a reduction in retention time of the DRAM devices. However, imec's 3D stacked demonstrator has proven that the DRAM may not be thermally isolated from the logic die since the DRAM die also acts as an effective heat spreader for the logic die. As such the intensity of the hot spot is reduced and thereby the temperature rise in the DRAM device is strongly limited.

The results of the various experiments allowed us to calibrate our thermal models which are implemented in 3D EDA tools. They have proven to be valuable means to design next-generation 3D stacked ICs. The design of the 3D chip is realized together with many players in the 3D integration supply chain.

"We are excited to achieve this milestone in collaboration with our 3D integration partners including memory suppliers and IC manufacturers. This test-chip and our 3D design tools and thermal models are an important step for the introduction of 3D technology in DRAM-on-logic for mobile applications;" said Luc Van den hove, president and CEO imec. "To boost the performance towards high-end applications, imec will set up a cooling research program."

This work was executed in collaboration with imec's key partners in its core CMOS programs Globalfoundries, INTEL, Micron, Panasonic,

Samsung, TSMC, Fujitsu, Sony, Amkor and Qualcomm.

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