

Toshiba's new technology cuts phase noise in oscillation ICs for wireless communication

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Toshiba Corporation today announced that it has developed noise reduction technology that reduces jitter in radio-frequency signals, cutting phase noise by up to 90 percent. This breakthrough opens the way for a further migration to high-speed wireless communication chips for wireless LAN and WiMAX.

Radio frequency phased locked loops (PLL) in [mobile communication](#) LSI chips were typically structured with analog and digital circuits. As achieving ultra-fine [analog circuits](#) is highly challenging, there is now a shift to all digital PLL using time-to-digital converters (TDC). While digitization reduces circuit size it also increases phase noise -- a degrading displacement in the pulse of a radio frequency signal -- due to larger delay in the TDC's inverter circuits. Cutting phase noise is essential for high speed communication standards, like WiMAX, which require highly accurate signals. There is the concern that current TDC is sensitive to variations in manufacturing processes that impact on their performance. This raises a need for more robust manufacturability.

To reduce susceptibility variations in mass production and suppress phase noise, Toshiba developed a new TDC integrating interpolation circuits that use a low resistance conductor to connect the output of two inverters. A triple interpolation splits the cycle of output signal of frequency synthesizers, and reduces phase noise by 90 percent. This solution successfully achieves a PLL with stable performance, as it utilizes a stable waveform from the PLL itself as a reference time interval for converting time to digital data, not the delay

time of the inverters. In a test chip manufactured with 65nm CMOS process, phase noise was reduced to -104dBc/Hz, 90 percent lower than that of the previous all digital PLL that Toshiba announced at ISSCC2011. Chip size was cut to 0.18 mm², approximately 80 percent smaller than the analog PLL in a mobile [WiMAX](#) transceiver chip that Toshiba announced at ISSCC2010.

This achievement will be announced on June 16 at the 2011 VLSI Symposium now being held in Kyoto, Japan.

Provided by Toshiba Corporation

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