Taiwanese group introduces new MorPACK, stacked chip

May 5 2011, by Bob Yirka

(PhysOrg.com) -- Taiwan's National Chip Implementation Center (CIC) has announced a new chip bundling design that they claim can cut development costs in half while also reducing the time it takes to bring a new chipset to market for a particular product, by as much as two thirds. Named the MorPACK, the chipset design uses a stacked approach, whereby newly designed chips can be stacked on top of existing processors (with air flow between them), reducing the space required to hold them, and increasing speed communication times between components as they are brought closer together.

In a paper submitted to *iMAPS*, author Shih-Lun Chen, of CIC, describes the structure of the MorPACK (short for morphing package) as a "heterogeneous integrated platform" of integrated parts that are put together as sort of building blocks, which allows the chipsets to require a smaller footprint. He also notes that due to the close proximity of the chips to one another in the stacked configuration, special care had to be taken to deal with heat issues; clearly something other's that wish to consider the chipset in their electronic devices will want to take a close look at as well.

The MorPack is built from the ground up; first, at the bottom is the processor, the biggest heat generator, which will likely sit atop a heat sink; above that are layer chips (connected by bridges) to provide linkage to memory chips, and then another to provide the same for peripheral devices. And then on top, come the custom chips designed by the companies that buy the MorPACK for use in their equipment.

Chiueh Tzi-dar, director general of the laboratory at CIC where the chip was designed, in interviews has stated that the MorPACK could be used for virtually any device that currently employs integrated chips; which of course would include all the consumer devices we've all grown used to; such as cell phones, cameras, etc. If this turns out to be true, all such devices could eventually be made even smaller than they are now due to the smaller footprint needed for the chipsets inside; though the current configuration of the MorPACK is 4 x 4 centimeters, project development leader Chun-ming Huang says he believes he and his team can reduce it to just a fourth that size, making it small enough to fit in devices as yet unimagined.

Citation: Taiwanese group introduces new MorPACK, stacked chip (2011, May 5) retrieved 28 June 2024 from https://phys.org/news/2011-05-taiwanese-group-morpack-stacked-chip.html