Imec and Atrenta develop exploration flows for 3D ICs

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Atrenta Inc., a leading provider of SoC Realization solutions for the semiconductor and electronic systems industries, in collaboration with imec's 3D integration IIAP (industrial affiliation program), have jointly developed an advanced planning and partitioning design flow for heterogeneous 3D stacked ICs. Imec and Atrenta will be demonstrating this flow at the Design Automation Conference (DAC) in San Diego, CA from June 6 – 8, 2011.

A flow allowing robust, accurate partitioning and prototyping early in the design process is critical to make cost-effective 3D systems and to get them to market fast. The flow under development allows minimizing the number of design iterations, facilitating a cost- and time-effective search of the solution space. Imec and Atrenta demonstrated their first EDA tool flow dedicated to 3D design exploration at last year's DAC.

3D stacked ICs are a promising technology for many designers. The main advantages are a reduced footprint with shorter and faster interconnects, increased system integration at a lower cost, and higher modularity and reuse. Examples of target applications include: products for mobile and high-performance applications, imagers, stacked DRAM, and solid-state drives.

To design innovative applications with 3D stacked dies, the ability to do early planning and partitioning is critical. The number of potential solutions for any given system design problem (e.g., front to front, front to back, silicon interposer, technology choice for slices, via

configurations, partitioning, etc.) is very large. Exploring this solution space through multiple full designs is simply too expensive and time-consuming. This makes it critically important to perform robust, accurate partitioning and prototyping early in the design process, well before detailed implementation begins.

There are other significant challenges for 3D design, such as the thermal profiles (heat dissipation) and the mechanical stress caused by assembly configurations. Imec has developed compact thermal and mechanical models for rapid generation of heat dissipation and mechanical stress maps and has validated them using real 3D DRAM-on-logic packaged devices. When combining the design floor plans produced by Atrenta's SpyGlass Physical 3D prototyping tool with the stress models developed by imec, different scenarios can be assessed quickly and the best option can be chosen in advance of a full design implementation.

Imec and Atrenta will be demonstrating the newest version of their advanced 3D planning and partitioning design flow in the Atrenta booth (1643) at DAC. The demonstration will include design partitioning across a 3D stack with routing congestion analysis, through silicon via (TSV) placement and backside redistribution layer routing support as well as display of thermal profiles on the 3D floor plan.

More information: For more information about Atrenta's demonstrations at DAC visit: www.atrenta.com/DAC2011/sessions_short.html

Provided by Imec

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