

Study: Error prevention, rather than correction, best for future of nanoelectronic devices

May 26 2011, By Wileen Wong Kromhout

The move toward smarter, lighter and more powerful electronics, computers and smartphones depends on whether transistor circuits, the building blocks of such devices, can process large amounts of information. As these circuits get faster and smaller, the number of errors they generate -- arising from heat dissipation, noise and structural disorder -- in the physical information they process increases, which can impede development.

Experts have debated which of two error-suppressing processes is more efficient and efficacious as these [circuits](#) are reduced to the nanoscale: (1) physical [fault-tolerance](#), in which the device is scaled down in size (and number of electrons) only to the point at which it can still prevent the generation of logical errors, or (2) architectural fault-tolerance, in which the device is continuously scaled down and robust algorithms are used to correct the errors it generates.

In a new study, Vwani Roychowdhury, professor of electrical engineering at the UCLA Henry Samueli School of Engineering and Applied Science and a member of the California NanoSystems Institute at UCLA, and Thomas Szkopek, professor of electrical and computer engineering at McGill University, and colleagues quantified for the first time these error-suppressing processes for model nanoelectronic systems and estimated the minimum number of electrons necessary for reliable circuit logic. They found that physical fault-tolerance in transistor

circuits suppresses the error rate per electron exponentially, while even the most efficient architectural fault-tolerance system only suppresses the error rate subexponentially. They conclude that physical fault-tolerance error prevention is better than architectural fault tolerance error correction.

The study contributes a fundamental insight into the reliability of nanoscale transistor device technologies and scaling and may impose a minimum limit on the size of devices. The findings are of immediate relevance to researchers working in transistor-scaling, through to scientists developing new device concepts.

More information: The research was recently published in the peer-reviewed *Physical Review Letters* and is available online at: prl.aps.org/abstract/PRL/v106/i17/e176801

Abstract

The error rate in complementary transistor circuits is suppressed exponentially in electron number, arising from an intrinsic physical implementation of fault-tolerant error correction. Contrariwise, explicit assembly of gates into the most efficient known fault-tolerant architecture is characterized by a subexponential suppression of error rate with electron number, and incurs significant overhead in wiring and complexity. We conclude that it is more efficient to prevent logical errors with physical fault tolerance than to correct logical errors with fault-tolerant architecture.

Provided by University of California Los Angeles

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