

Elpida develops industry's first 25nm process DRAM

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Elpida Memory, Japan's leading global supplier of Dynamic Random Access Memory (DRAM), today announced it had developed a 2-gigabit DDR3 SDRAM using an industry-leading 25nm process for memory manufacturing. Using the most advanced process technology available Elpida has achieved the industry's smallest chip size for a 2-gigabit SDRAM.

The newly developed 25nm DRAM process technology requires 30% less cell area per bit compared with Elpida's 30nm process. The chip output for a 2-gigabit DDR3 SDRAM [wafer](#) using the new process is about 30% higher versus 30nm.

The new SDRAM is an eco-friendly as it contributes to lower [energy consumption](#) by PCs and digital consumer electronics. It outperforms Elpida's 30nm process products by saving on electric current (15% less operating current and 20% less current when on standby).

At the time the 25nm process was developed the structural changes required to shift from a 30nm process were minimized to hold down the capital expenditure needed for ramping up 25nm volume manufacturing.

By the end of 2011 Elpida also plans to begin volume production of 4-gigabit DDR3 SDRAM products using the 25nm process. Compared with the 30nm process a 44% increase in chip output per wafer is expected for this 4-gigabit DDR3 product. In addition, the new 25nm process will be used to support further development of Mobile RAMTM,

Elpida's mainstay [memory](#) product.

The 25nm process 2-gigabit DDR3 SDRAM can support ultra-fast performance above DDR3-1866 (1866Mbps) and is compliant with low-voltage 1.35V high-speed DDR3L-1600 (1600Mbps).

Both sample shipments of the new 25nm 2-gigabit [DDR3 SDRAM](#) and volume production are expected to begin in July 2011.

Source: Elpida

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