Researchers advance design-dependent process monitoring for semiconductor wafer manufacturing

May 25 2011

Semiconductor Research Corporation (SRC), the world's leading university-research consortium for semiconductors and related technologies, and researchers from the UCLA Henry Samueli School of Engineering and Applied Science have developed a new method of design-dependent process monitoring for semiconductor wafer manufacturing. The advance promises to provide semiconductor chip manufacturing cost and productivity savings up to 15 percent, potentially increase profit per chip by as much as 12 percent and ultimately lead to less expensive and higher performing electronics devices.

The complexities of semiconductor manufacturing and the challenges of keeping pace with Moore's Law are well known within the industry. Modern manufactured chips exhibit wide power and performance variation that necessitate careful screening, and frequency and power tests to screen for defective chips after chip packaging has been completed are expensive and time consuming.

Therefore, the industry has significant incentive to prune failed wafers and chips during early stages of manufacturing wherever possible. While increased attention has been given to the design-manufacturing interface, little has been done to drive design intent into manufacturing.

That's where UCLA Engineering research comes into play. By using process monitors on wafer lines tested after the initial manufacturing

steps, manufacturers would be able to evaluate early die performance and wafer yield estimation. Avoiding going through all the manufacturing steps for a bad wafer can realize the significant cost savings. Avoiding testing failed die later in the process by leveraging the pruning approach is expected to save manufacturing costs further, with nearly 70 percent of failed chips pruned with less than a 1 percent yield loss. Though the results will depend on the design as well as the manufacturing process, the approach is especially useful in early stages of yield ramp for a product. An early version of this work appeared in the International Conference on Computer-Aided Design in 2010.

"The notion of design-assisted manufacturing is a big change from the way things are done currently," said Puneet Gupta, professor of electrical engineering at UCLA who is also a SRC alumni student. "Our research provides the industry a way to not waste resources in producing silicon wafers that will eventually lose money because chips on them are not good enough for production. We believe that the cost reductions from this and other design-assisted manufacturing methods that we are investigating could easily be as much as one full technology node."

Along with semiconductor foundries, design houses would also benefit from wafer-cost reductions achieved through the design-dependent process monitoring approach. Researchers are fine-tuning the approach-including finalizing results from a 45 nanometer silicon prototype effort-and hope to see the industry begin implementing the process within the next few years.

"The semiconductor industry has been heavily focused on purely technological solutions to scaling, and we've barely scratched the surface on the potential of design-assisted technology scaling," said Bill Joyner, SRC director of Computer-Aided Design and Test. "This research leverages design information meaningfully and practically to reduce process control requirements and manufacturing costs."